Master Thesis

Thesis in Electronics, 15 credits

Enhancing Sustainability Through Test Point Optimization in PCBA Production Testing

Master's Programme in Electronics Design, 60 credits

Halmstad August 18, 2025

Aparna Mahendran

Elon Anne Benny

HALMSTAD UNIVERSITY

Abstract

This thesis explores the principles of circular economy in production test environment, aiming to enhance sustainability without sacrificing product quality. Focusing on Printed Circuit Board Assembly (PCBA) testing, the study investigates four key areas: modular and reusable Bed-of-Nails (BoN) fixture designs; dynamic power management using smart relays; alternative test methodologies; and test-point optimization based on schematic analysis and historical failure data.

Through a detailed review of eight commercial PCBA designs and associated yield records, the research demonstrates that approximately 30% of existing test points can be removed without diminishing diagnostic effectiveness resulting in simpler fixtures and shorter test cycles. Modular fixtures present advantages in terms of material efficiency and reusability. However, their adoption within Electronics Manufacturing Services (EMS) is limited by the high initial engineering requirements, lack of standardized interfaces, and the necessity for operator training. Although smart relay based power gating is technically implementable, it offers limited economic incentives under prevailing energy rates. Similarly, Boundary Scan and Flying Probe Testing provide valuable flexibility for small-batch and prototype testing but cannot match the throughput of optimized fixture-based methods in high-volume production.

Based on the research outcomes, this thesis proposes actionable engineering strategies, including the prioritization of test points, the standardization of modular fixture designs, and the implementation of targeted power management approaches aimed at embedding circular economy concepts into end-of-line testing processes. By doing so, it advances UN Sustainable Development Goal 12.5, driving down electronic waste, preserving valuable resources, and strengthening the durability of test-system infrastructure.

Acknowledgements

We would like to express our sincere gratitude to the entire **Industrialization Production & Test EVP team** at **Axis Communications, Lund**, for their generous support, collaboration, and commitment throughout the course of our project. Your willingness to share your time, expertise, and insights significantly enriched our learning experience and contributed to the success of our work. The positive and collaborative environment you fostered made our journey both productive and truly enjoyable.

We are especially grateful to our manager **Anders Svensson** and supervisor **Artur Matusiak** for their exceptional guidance, technical expertise, and continuous encouragement. Your dedication, enthusiasm, and belief in our potential played a pivotal role in motivating us and driving our progress forward. Your mentorship was not only technically invaluable but also personally inspiring, and we deeply appreciate the thoughtful guidance and encouragement you provided throughout our journey.

We would also like to extend our heartfelt appreciation to **Anders Sjö**, **Tommy Nordin**, **Deshane Davis**, and **Philip Damberg** for their invaluable contributions and hands-on support during the most essential phases of the project. Your willingness to engage, offer practical solutions, and share your deep domain knowledge had a profound impact on our ability to navigate challenges effectively.

A special word of thanks to **Aishwariya Ramachandran** for her constant encouragement, approachability, and uplifting presence. Your positivity and support made our experience more memorable and meaningful.

Lastly, we are deeply thankful to our academic supervisor, **Dr. Pererik Andreasson**, for his steady guidance and thoughtful feedback throughout the project. His academic insight and mentorship were integral to our development and the successful completion of our work.

We are truly grateful to everyone who has been part of this journey. Thank you for making our time at **Axis Communications** a rewarding and inspiring experience.

Contents

Abstract . . . . . **iii**
Acknowledgements . . . . . **v**
Contents . . . . . **vii**
List of Figures . . . . . **ix**
List of Tables . . . . . **xi**
1 Introduction **1**
1.1 Background 1
1.2 Problem Statement 2
1.3 Purpose 2
2 Technical Background **5**
2.1 Bed of Nails Test 6
2.1.1 Test Fixtures 6
2.1.2 Test Points 8
2.1.3 Test Pins 9
2.2 Test Station 10
2.2.1 Spider 11
2.2.2 Cisco Switch 11
2.2.3 Data Acquisition / Data logger Switch 11
2.2.4 RME Sound Card 11
2.3 Boundary Scan 13
2.4 Flying Probe Testing 15
3 Literature Review **17**
3.1 Rethinking Test Fixture Design: From Dedicated to Modular 17
3.2 Energy Efficiency through Intelligent Test Station Management . . . 18
3.3 Boundary Scan: Virtualizing Physical Access 18
3.4 Test Point Optimization: Doing More with Less 19
4 Methodology **21**
4.1 Development Process 21
4.1.1 Modular Test Fixture Designs 21

4.1.2 Alternative Testing Methods-To Reduce The Count of Test Points . . . 23
4.1.3 Power Optimization Using Smart Relays . . . 24
4.1.4 Test points optimization . . . 25
5 Results . . . 29
5.1 Idle-State Power Consumption Analysis of the Test Stations . . . 29
5.2 Failure Pattern Analysis in PCBA designs . . . 30
5.2.1 Fixed Dome Camera . . . 30
5.2.2 Multisensor/multidirectional Camera . . . 31
5.2.3 Dual-head Camera . . . 32
5.2.4 Panoramic Multisensor Camera . . . 33
5.2.5 Modular Camera . . . 34
5.2.6 Fixed Mini-Dome Camera . . . 35
5.2.7 Bullet Camera . . . 35
5.3 Proposed Strategies for Test Point Optimization . . . 36
5.4 Guidelines for Sustainability in Production Test Environments . . . 40
6 Discussion . . . 43
6.1 Societal aspects . . . 44
6.2 Future work . . . 44
6.3 Conclusions . . . 45
Bibliography . . . 47
A Survey Feedback . . . 51
A.1 Key Challenges in Implementing Sustainable Practices . . . 51
A.2 Recommendations for Enhancing Sustainability in Test Areas . . . 52
A.3 Additional Observations and Ideas . . . 53

List of Figures

2.1 Customized Test Fixture by Promoco [4]. 7
2.2 Test point in a PCBA [7]. 8
2.3 A render of an Ingun test probe showing the barrel (1), spring (2), probe (3), and tip (4). [8] 9
2.4 Test-setup for PCBA Testing 12
2.5 Basic Boundary Scan Cell [11] 13
2.6 IEEE 1149.1 Chip Architecture [11] 14
2.7 Flying Probe Testing [15] 15

4.1 Modular Test Fixture designed by Promoco 23
4.2 Block diagram for Smart Relay approach 25

5.1 Test points vs Yieldloss/Error for Fixed dome camera 31
5.2 Test points vs Yieldloss/Error for Multisensor/multidirectional cameras 32
5.3 Test points vs Yieldloss/Error for Dual-head camera 33
5.4 Test points vs Yieldloss/Error for Panoramic Multisensor Camera . . 33
5.5 Test points vs Yieldloss/Error for modular camera 34
5.6 Test points vs Yieldloss/Error for fixed mini-dome camera 35
5.7 Test points vs Yieldloss/Error for Bullet camera 36
5.8 Schematics of TB6612FNG using KiCad 37
5.9 Block Diagram for Temperature sensor 38
5.10 Schematics of H-bridge motor drivers after TP optimization 39

List of Tables

A.1 Historical failure rate of Test points in Fixed Dome Camera 54
A.2 Historical failure rate of Test points in Multisensor/Mutli-directional Camera 56
A.3 Historical failure rate of Test points in Dual-Head Camera 57
A.4 Historical failure rate of Test points in Panoramic Multisensor Camera 58
A.5 Historical failure rate of Test points in Modular Camera 59
A.6 Historical failure rate of Test points in Fixed Mini-Dome Camera . . 60
A.7 Historical failure rate of Test points in Bullet Camera 61

Chapter 1

Introduction

As global competition increases, companies are expected to showcase their commitment to sustainable development in its operations by evaluating and developing sustainable practices.United Nations has introduced Sustainable Development Goals (SDG) to create a better and sustainable future for all. The UN Sustainable Development Goals are 17 global targets to create a fair, healthy, and sustainable world for present and future generations [1]. Sustainability can be beneficial to businesses as it often provides a competitive edge. It can also help them reach more customers and grow their market share. On top of that, it can lead to better value for shareholders. Reaching this goal involves putting strategies and actions in place that thoughtfully address the current needs of stakeholders. It supports the preservation and growth of human and environmental resources for the benefit of future generations. To support such evaluations, it is crucial to establish a solid framework with clear criteria and meaningful indicators for measuring sustainability within the industry.

This thesis focuses on analyzing existing practices in the production testing environment and exploring ways to make them more sustainable. While speed and innovation are crucial for maintaining a competition among companies, there is a growing acknowledgement that these factors must be balanced with sustainability objectives.

1.1 Background

Electronics manufacturing demands the use of precious metals and hazardous materials. It produces significant carbon emissions that add to global warming. On top of that, electronic waste is becoming a serious problem. Innumerable electronic devices are discarded yearly, which release harmful toxins into the environment. This research explores how the electronics industry can align with the Sustainable Development Goals (SDGs), with a focus on SDG 12.5, which emphasizes for a substantial reduction in waste by 2030 through measures like pre-

vention, reduction, recycling, and reuse. Promoting sustainability in this sector is crucial to safeguard the planet's future [2]. Embracing sustainable methods allows the industry to lessen its ecological footprint, conserve essential resources, and contribute to a healthier planet for the generations to come. As technology continues to evolve, it is crucial that progress aligns with principles of sustainable development.

1.2 Problem Statement

This thesis investigated multiple factors in the production test environment that influence sustainability.

- Investigate the possibility of using modular test fixture designs for Bed-of-Nails (BoN) testing to improve material efficiency and minimize design redundancy.
- Quantify the idle state power consumption and evaluate the implementation of smart relay technology to achieve power efficiency improvements.
- Perform a comprehensive evaluation of multiple PCBA testing approaches to assess their effectiveness in supporting sustainability.
- Propose design-level optimizations to minimize the number of test points without compromising test coverage or product quality.

Establish guidelines to facilitate the implementation of sustainable testing strategies in production test environments, ensuring alignment between electronic design processes and long-term environmental objectives.

1.3 Purpose

There is a persistent sense of demand associated with bringing new products to market, often at the expense of environmental responsibility. The main purpose of this study is to identify the most valuable aspects of the circular economy that can be integrated into the PCBA test environment. This involves evaluating the trade-offs between environmental benefits and the commercial implications of potential changes such as less power consumption, alternative testing methods and a standardized test procedure.

When PCBA testers define test points in the bed of nail fixtures, it must be clear that this test will have a significant value for Axis. Including less priority test points or redundant test points will increase the complexity of customized bed of nails fixtures. A key objective is the optimization of test points in PCBA testing to enhance both sustainability and test coverage. The research involves analyzing test schematics and historical test data to identify critical, optional, and redundant nets with the aim of eliminating those points that do not compromise

test effectiveness. Nets that consistently show low failure rates can be targeted for elimination, helping to steamline the testing process and reduce unnecessary use of resources.

In addition to improving test point efficiency, the research explores ways to physically reuse components of test fixtures. This involves implementing modular designs in place of custom-built fixtures and repurposing the mechanical frames of existing setups. Such strategies help extend the life of components, minimize material waste, and align with environmental objectives while also offering long-term cost reductions and enhanced operational performance.

Chapter 2

Technical Background

Production testing is a structured and automated process that is used to evaluate every unit of an electronic assembly during manufacturing. Its main purpose is to confirm that each unit meets expected design requirements and functions. In large-scale electronics production, especially in Printed Circuit Board Assembly (PCBA), this testing plays a critical role in identifying faults that may occur during component placement, soldering, or handling. This testing phase typically integrates various methodologies, including In-Circuit Testing (ICT) for electrical continuity and component verification, Flying Probe Testing for low-to-medium volume flexible probing without requiring custom fixtures, and Functional Circuit Testing (FCT) to validate system-level behavior under operational conditions.

Advanced techniques like Boundary Scan (JTAG) can be used to access and test densely packed integrated circuits, especially in designs featuring BGA packages where physical probing is limited. Automated Optical Inspection (AOI) systems are deployed for non-contact visual verification of solder joints and component orientation. In certain scenarios, Burn-In Testing is utilized to detect early component failures by subjecting devices to extended thermal and electrical stress. The use of such testing techniques enhances overall test coverage, aids in statistical process control, and helps maintain low defect levels during manufacturing. Furthermore, production testing is closely tied to Design for Testability (DFT) principles, which improve testing efficiency by incorporating test points, diagnostic interfaces, and modular system designs. Together, these approaches ensure that only fully functional and reliable units move forward to final packaging and shipment.

A PCBA, represents a circuit board that has been fully populated with electronic components. It forms the functional core of most electronic devices by enabling electrical connections and supporting component operation. PCBA testing is done to find problems before a product ever gets into a customer's hands. Technicians go through each part of the circuit board to make sure everything works just the way it's supposed to. They use specialized tools and software to check

things like electrical signals, power levels, and data flow. It's a key step in making sure the final product is reliable and high quality. PCBAs serve as the core of electronic gadgets. However, to ensure these intricate parts are operating correctly, PCBA test fixtures are used.

2.1 Bed of Nails Test

The bed-of-nails test is one of the common approaches for testing the performance and quality of PCBAs. It consists of a fixture equipped with spring-loaded probes. When PCBAs are connected to the fixture, these probes make contact with specific test points on the circuit board.

Bed-of-nails are customized to align with the design of the PCBAs that have to be tested, and each of these pins is pressed against the test points. This will help in measuring electrical signals in the corresponding nets [3]. This allows the testing system to identify short circuits, broken circuits, and other production flaws that could impact the product's functionality. Bed-of-nails testing facilitates quick assessment of numerous test locations at the same time, providing effective testing of substantial quantities of PCBs or electronic devices. The test setup guarantees reliable and replicable testing across various units, by increasing the possibility of finding errors before the product leaves the factory. This can be customized to accommodate various PCBA designs and testing criteria and are adaptable across various applications.

2.1.1 Test Fixtures

End-of-line (EOL) testing is a key process in the final phase of electronics production. It validates the functional integrity of each unit, confirming compliance with performance specifications before delivering to customers. Identifying faults at the final stage of production helps verify operational integrity and compliance with design specifications. Early identification and resolution of issues significantly reduces the risk of costly rework, warranty claims, or product recalls, ultimately saving time, resources, and safeguarding brand reputation. These tests help to detect the presence of short circuits, confirm that component values meet design specifications, and ensure that essential components, such as Microcontroller Units (MCUs) are functioning correctly.

PCBAs which form the core of modern electronic devices, demand comprehensive end-of-line testing due to their complexity. This validation process is vital to answering critical quality assurance questions before product integration or shipment. To facilitate this process, PCBA test fixtures are employed. A test fixture is a precision-engineered mechanical and electrical interface used to perform consistent and repeatable testing on PCBAs. Figure 2.1 shows the test fixture designed by Promoco. It securely holds the Unit Under Test (UUT) in place and establishes

reliable electrical contact with designated test points, pads, connectors, or boundary scan interfaces. In both In-Circuit Testing (ICT) and Functional Circuit Testing (FCT), fixtures commonly utilize spring-loaded pogo pins to access internal nodes, power rails, and digital lines without damaging the board. Test fixtures may be customized for specific board layouts and often incorporate embedded wiring, relays, load emulation circuits, and protective features such as ESD shielding and current limiting.

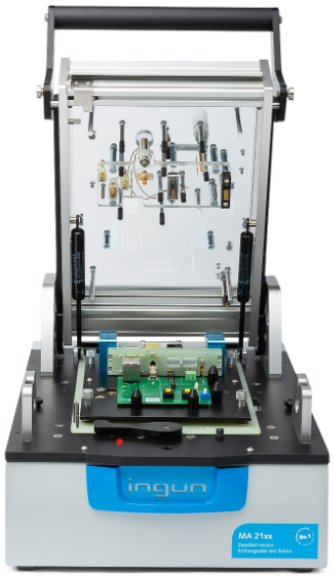


Figure 2.1: Customized Test Fixture by Promoco [4].

Advanced fixtures can include automated features such as mechanical actuators, clamping systems, and modular interfaces, which streamline the test process and minimize operator intervention. Effective implementation of test fixtures is supported by Design for Testability (DFT) principles, which focus on the inclusion of test points, alignment holes, and standardized connectors during the PCB layout phase. These considerations ensure test coverage is maximized while maintaining manufacturability and throughput efficiency. Apart from the DUT, electronic testing also consists of the test equipment and test fixture. One challenge for test engineers is managing the complexity of measuring hundreds or thousands of electrical nodes through a reliable mechanical interface. This complexity necessitates precise fixture design and robust signal routing to ensure test integrity and accuracy.

While manual testing methods such as programming and probing PCBs with measurement instruments are accessible and involve low initial cost, they are not scalable. Large-scale manufacturing can't be done manually because of the higher time consumption and unreliable outcome. Functional Circuit Test (FCT) fixtures,

on the other hand, offer a fast, reliable, and easily scalable alternative. In contrast, FCT fixtures provide a scalable, high-speed, and accurate testing solution. While FCT fixtures require considerable initial investment in custom hardware and engineering resources, they significantly decrease the time needed for testing. Once implemented, a functional test fixture can typically execute a complete test cycle in approximately five minutes or less, representing a significant efficiency gain over manual methods. In conclusion, production testing, particularly at the end-of-line, plays a vital role in ensuring the quality of PCBAs. The use of test fixtures streamlines this process and enhances test coverage, repeatability, and efficiency. For manufacturers seeking to balance quality assurance with production scalability, fixture-based testing remains an indispensable approach.

2.1.2 Test Points

A test point on a PCB is a predefined access location that is used to apply test signals and measure the electrical parameters to verify the functionality, connectivity, and integrity of the circuit. Figure 2.2 shows Test points in a PCBA. These points are typically placed along signal traces or near component leads to facilitate testing during both production and development phases [5]. They verify that components adhere to design requirements and aid in detecting faults like open circuits, shorts, or soldering defects. Beyond production testing, test points are crucial for debugging and maintenance, allowing engineers to quickly isolate and resolve faults. Test points also serve as access points for diagnostic tools. It helps engineers pinpoint and address issues quickly during the debugging and troubleshooting phases [6]. Test points on printed circuit boards are crucial for confirming their performance and quality. Test points are precisely designed and placed to optimize testing and safeguard critical systems.

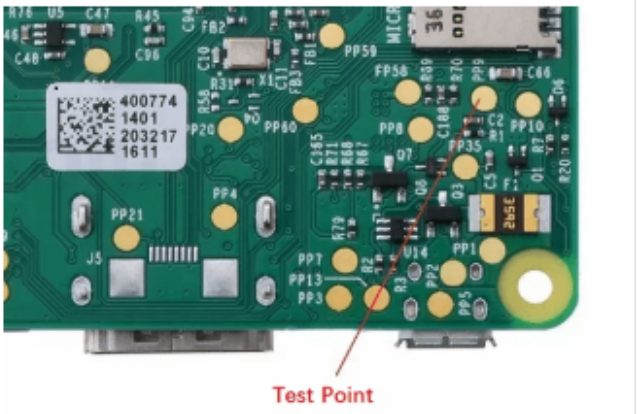


Figure 2.2: Test point in a PCBA [7].

When designing PCB test points, multiple factors must be evaluated to achieve effective and reliable testing:

- Identify critical test locations, such as power and ground planes, signal paths, and component interfaces, to determine where test access is essential.
- Strategically place test points in accessible areas, ensuring they are not obstructed by other components and can be reached by test probes or automated testing equipment.
- Select the appropriate test point type, such as surface-mount pads, test loops, or through-hole points based on the PCB layout and specific testing requirements.
- Clearly label each test point with standardized identifiers (e.g., GND for ground, VCC for power) to aid in debugging and test automation.
- Make sure that test points are placed in a way that preserves signal integrity and avoids introducing additional inductance or capacitance that could impact electrical performance.
- Design test points for durability, especially in automated test setups, where they must withstand repeated mechanical contact without wear and tear.

This approach ensures that the PCB remains testable, reliable, and compliant with both functional and production-level testing standards.

2.1.3 Test Pins

A bed-of-nails fixture is a platform equipped with multiple spring-loaded pogo pins arranged to correspond to the layout of a particular PCBA. These fixtures allow signal injection and response monitoring to confirm proper operation of the board and its components when paired with automated test equipment(ATE). Fixtures are individually designed to match the PCBA design to ensure reliable access to all required test points. Figure 2.3 shows a render of an Ingun test probe showing different parts. When the fixture is closed, the pins make contact with these points to enable electrical testing. Each pin has a needle inside a cylinder, with a spring adding force to create a solid link. The pin's end is usually sharp or curved to ensure it connects well with the test spot.

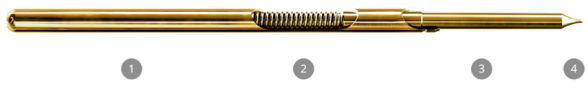


Figure 2.3: A render of an Ingun test probe showing the barrel (1), spring (2), probe (3), and tip (4). [8]

Each spring-loaded pin features a plunger inside a barrel, using a spring to exert force and ensure a secure connection. The plunger's end is usually pointed or rounded to guarantee dependable contact with the point being tested. Spring-loaded pins are commonly used because of their longevity and stable contact pressure, which make them ideal for repeated engagement in test environments. They are available in multiple sizes and tip shapes to suit different testing area dimensions and concentrations.

Receptacles are elements designed to hold spring-loaded test probes. They are generally fitted into the probe plate of the testing apparatus. Receptacles make it simple to swap out test probes if they are broken or reach the end of their lifespan, which increases the longevity of the test fixture. They also offer a firm base for the test probes, which guarantees reliable positioning and contact with the test locations on the circuit board.

2.2 Test Station

A PCBA Test Station is a specialized automated system designed to validate the electrical response, signal integrity, and assembly quality of printed circuit board assemblies during or after the manufacturing process. These stations are typically equipped with test fixtures (bed-of-nails, flying probes, or custom jigs), measurement instruments (oscilloscopes, multimeters, logic analyzers), and programmable power supplies, all controlled by test automation software. The testing process ensures the PCBA adheres to the intended design, detects manufacturing faults early, and provides traceable data for quality control. Integration with MES (Manufacturing Execution System) allows for automated logging of test results, defect tracking, and statistical yield analysis. Figure 2.4 shows the Test-setup for PCBA Testing. It allows for prompt decisions and continual refinement of operations. The test station consists of:

- Spider - Axis global production system
- Cisco Switch - Managed Ethernet switch
- TTI QL564P Power Supply - Precision programmable linear power supply
- Keysight E3645A Power Supply - Single-output programmable DC power supply
- Keysight 34970A DAQ - Data acquisition/switch unit with embedded Digital Multimeter [9]
- RME Sound card - High-end audio interface for professional recording and playback

2.2.1 Spider

The production system used by Axis is called Spider. It is used to assemble, test, program, and package products in the manufacturing facilities before they are shipped. Spider is used in PCBA testing, Sub-Assembly (SA) testing, Unit Assembly (UA)/ Product Unit (PU) Testing and Packing. It runs in all Axis manufacturing and logistics facilities worldwide and interacts with all units multiple times during production.

2.2.2 Cisco Switch

The Cisco Switch is a reliable and high-performance network device used to manage and route data traffic efficiently between multiple devices in a test station environment. The Cisco switch plays a crucial role in establishing stable Ethernet connectivity between test equipment, computers, and the devices under test (DUTs) such as network cameras or intercom units. It supports multiple VLAN configurations, enabling isolated network segments for simultaneous testing without interference. The switch ensures high-speed data transfer, low latency, and consistent packet delivery, which are essential for real-time video and audio testing. Its robust management interface allows network engineers to monitor, control, and troubleshoot connectivity issues in the test setup, thus contributing to an efficient and scalable test environment.

2.2.3 Data Acquisition / Data logger Switch

Generally, data acquisition (DAQ) systems can handle both changing and constant measurements, enabling them to sample at both fast and slow rates. These systems typically include or are linked to a powerful computer and provide advanced signal processing, allowing connection to numerous sensors. Most common DAQ systems have channels ranging from 8 to 16 and are used for short duration testing. DAQ systems are used for short duration tests. The higher cost is mainly due to the greater durability of their signal conditioners. These instruments are capable of handling dynamic as well as static or quasi-static signals and often feature higher sampling rates. DAQ systems have storage capacities ranging from gigabytes to terabytes.

Axis uses Keysight 34970A DAQ for its test stations. Each channel can be set up separately to measure one of 11 varied functions, and no signal-conditioning add-ons are required.

2.2.4 RME Sound Card

The RME sound card functions within automated test systems to provide precise latency control together with high-fidelity audio input/output capabilities.

The system provides exact signal generation and measurement capabilities when conducting audio hardware and software tests. The test station integrates RME sound cards to generate high-quality audio signals while simultaneously capturing them to evaluate surveillance devices, including network cameras and intercom systems. The system delivers exact playback and recording of audio signals, which makes it vital for testing microphone sensitivity and speaker output levels and overall audio quality in controlled test settings. The test results become consistent and reproducible because of the sound card's ASIO driver support and high signal-to-noise ratio, making it essential for automated and manual test operations. The integration between measurement software allows audio testing to occur in unison with broader hardware validation processes.

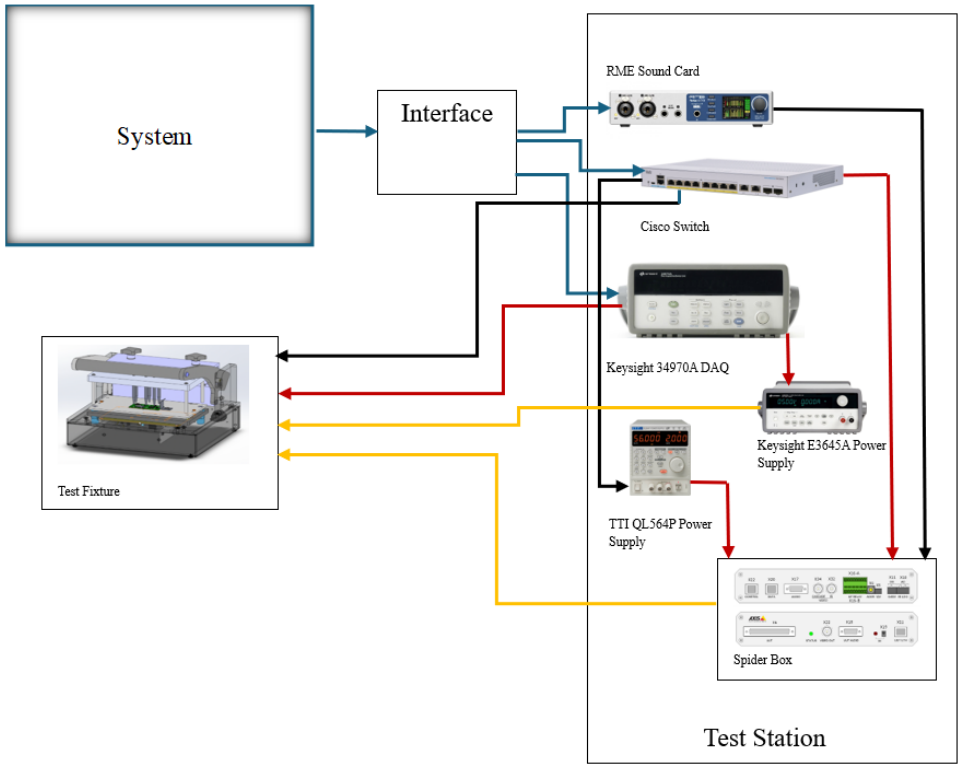


Figure 2.4: Test-setup for PCBA Testing

2.3 Boundary Scan

Boundary Scan, based on IEEE 1149.1 / JTAG, enables testing of interconnects and internal logic at the IC level without physical test access. In Boundary scan, a serial shift register is placed around the boundary of the device. Figure 2.5 illustrates the architecture of an IEEE 1149.1 chip. Each primary input and primary output signal is supplemented by a multi-purpose memory element known as a boundary-scan cell [10].

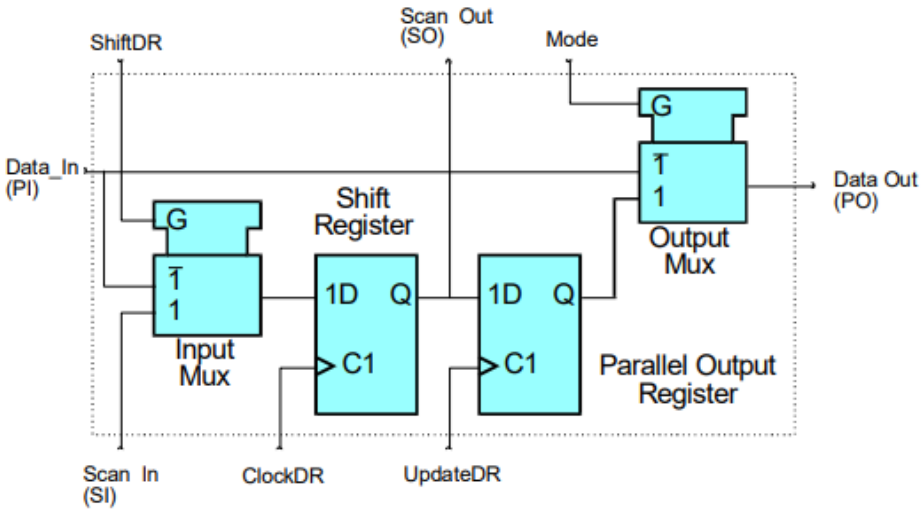


Figure 2.5: Basic Boundary Scan Cell [11]

These boundary scan cells are connected to form a parallel-in, parallel-out shift register. A capture operation copies signals from the input pins of the device into the input cells and from the core logic to the output pins into the output cells. An update operation transfers the contents of the output scan cells to the device output pins. Depending on the configuration of the input scan cells, values stored in them may also be passed into the device's core logic.

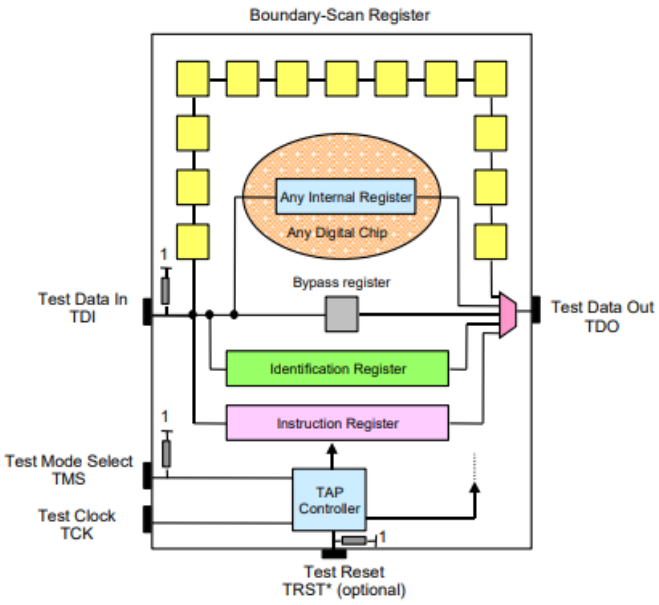


Figure 2.6: IEEE 1149.1 Chip Architecture [11]

Figure 2.6 shows the following elements [11]:

- A set of four dedicated test pins — Test Data In (TDI), Test Mode Select (TMS), Test Clock (TCK), Test Data Out (TDO) and one optional test pin Test Reset (TRST). These pins are all called the Test Access Port (TAP).
- A boundary-scan cell is placed on each main input and output pin of the device, and they are connected internally to form a serial boundary-scan register (Boundary Scan).
- A TAP controller, which is a finite-state machine, with TCK, TMS, and TRST as its inputs.
- An n-bit (n>=2) Instruction Register (IR), used to hold the current instruction.
- A 1-bit bypass register (Bypass).
- An optional 32-bit Identification Register (Ident) that can be programmed with a permanent device identification code.

Data can also be shifted serially through the shift register, starting from a dedicated input pin called Test Data In (TDI) and exiting through a dedicated output pin called Test Data Out (TDO). A separate clock signal, Test Clock (TCK), is fed into each device, while the mode of operation is controlled by a dedicated serial control signal known as Test Mode Select (TMS) [12]. Using boundary-scan cells to test the core logic of a device is referred to as Internal Test (Intest), while using them to test interconnects between devices is known as External Test (Extest). Extest is the primary application of boundary-scan architecture, used to detect open circuits, shorts, and damage at the device periphery. Intest is typically lim-

ited to simple checks such as verifying presence, orientation, and alignment of the device [13].

2.4 Flying Probe Testing

Flying Probe Testing (FPT) utilizes flying probe analyzers, which are advanced, fixture-less test systems equipped with precision robotic arms that move conductive probes across a PCB surface. These analyzers operate under software control to access electrical nodes, such as pads, vias, and component leads, based on imported design data like Gerber files or netlists. Figure 2.7 provides a visual representation of Flying Probe Testing. Flying probe analyzer performs a variety of in-circuit electrical tests such as continuity, isolation, resistance, and capacitance without powering the board [14]. This non-invasive, non-powered testing helps detect defects like opens, shorts, and incorrect soldering without risking damage to sensitive components. Some advanced analyzers may also include optional vision systems or optical inspection modules for alignment and component verification.

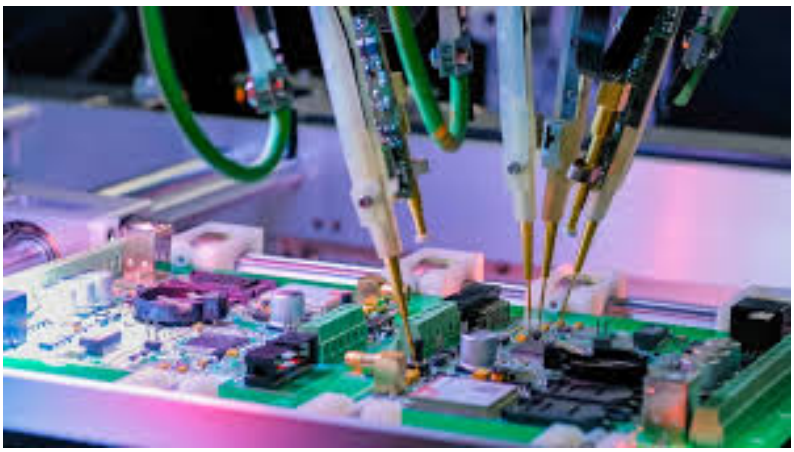


Figure 2.7: Flying Probe Testing [15]

A key advantage of the flying probe analyzer is its versatility and low setup cost. Since it does not require a custom test fixture, it is ideal for prototype validation, small-batch production, and engineering change evaluations. The analyzer allows for rapid test development, easy test plan modification, and excellent access to densely packed or complex PCB layouts. It is especially useful in research and developments areas and failure analysis environments, where flexibility and precision are more critical than speed. Moreover, modern flying probe analyzers can test both sides of a board and support simultaneous multi-probe contact, improving test efficiency over single-probe systems [16].

Chapter 3

Literature Review

As electronics manufacturing becomes more complex and resource-intensive, circular economy policies replace the existing one-way production and disposal. In production settings, especially within electronic testing, rapid product turnover, component discontinuation, and accelerated innovation cycles are prevalent. Implementing a circular model can yield considerable benefits for both the environment and operational efficiency.

The circular economy prioritizes on designing systems for durability, reuse, adaptability, and minimal waste. Within the context of production testing, this translates into creating test infrastructures that are modular, reconfigurable, and software-driven rather than rigid, single-use hardware setups. By reducing fixture duplication, optimizing energy use, and minimizing material demand through smarter testing methods, the testing itself can become a contributor to a product's sustainable lifecycle.

Based on the survey that was conducted among PCBA and DFT engineers, this work focuses on four interrelated themes: reconfigurable and modular test fixtures, energy-efficient test station operation, boundary scan testing, and test point optimization.

3.1 Rethinking Test Fixture Design: From Dedicated to Modular

Traditional bed-of-nails fixtures have been widely used in in-circuit testing (ICT) and functional circuit testing (FCT) in high-volume production environments. It uses spring-loaded probes to make contact with the test points. Despite their effectiveness, such fixtures are highly customized to specific board layouts, resulting in significant material waste and recurring engineering effort when adapting to new designs. Recent advancements in modular and reconfigurable fixture systems represent a notable shift in testing methodology.

As demonstrated in the work of Bejlegaard et al. [17], reconfigurable architectures allow a single fixture to accommodate testing for multiple subcomponents up to 14 in their study by enabling structural and functional adjustments. This flexible approach reduces the need for multiple unique fixtures, leading to decreased storage requirements, shorter setup times, and lower production costs. In addition, it supports wider sustainability goals by promoting fixture longevity, reuse, and adaptability, aligning with principles of circular economy and reducing environmental impact.

3.2 Energy Efficiency through Intelligent Test Station Management

Energy efficiency in production testing can be significantly enhanced through intelligent test station management. In conventional setups, test stations which are powered during idle periods consumes unnecessary power. Recent studies highlight the use of smart relays and programmable logic to monitor station activity and dynamically control power distribution [18]. By detecting periods of inactivity such as during shift transitions or board changeovers these systems can automatically initiate standby modes or disconnect power to unused equipment. This approach helps lower energy consumption as well as supports sustainability efforts by reducing the total carbon footprint associated with the testing process [19]. The integration of such intelligent energy management strategies aligns with broader Environmental, Social, and Governance (ESG) objectives, offering a scalable solution for improving resource efficiency in high-mix, low-volume manufacturing environments.

3.3 Boundary Scan: Virtualizing Physical Access

The IEEE 1149.1 boundary scan standard or JTAG, provides an interface that can be accessed by software for testing interconnects and internal circuitry within digital devices. This standard significantly reduces the need for physical test points, an increasingly important advantage as printed circuit boards (PCBs) become more compact and densely populated [20]. Initially developed to address the accessibility limitations inherent in surface-mounted devices, boundary scan has since become a widely adopted method in modern electronics testing and manufacturing. It enables a range of testing and diagnostic functions, including board-level interconnect verification, in-system programming, and power-on diagnostics all with minimal reliance on physical fixtures [21]. By shifting test coverage from hardware to software, boundary scan supports sustainable engineering practices, such as reducing fixture wear, enhancing component reusability, and enabling software-driven updates, thus aligning with circular economy goals [22].

3.4 Test Point Optimization: Doing More with Less

Test point optimization involves minimizing the number of physical access points on a PCB while ensuring sufficient coverage for quality assurance. This approach supports miniaturization, reduces test fixture complexity, and enhances product reliability, all vital to sustainable process control.

A compelling case is presented in the work of Williams, who proposes a structured approach to system-level test coverage modelling is proposed to address the challenges of verifying complex systems where individual components have already undergone separate testing [23]. The paper outlines two key strategies for optimizing test coverage. The first involves creating a multi-tiered fault model encompassing chip, board, and system levels, allowing simulated evaluation of test effectiveness though this method depends heavily on detailed and accurate fault data.

The second, more practical approach applies Failure Mode and Effect Analysis (FMEA) to categorize faults based on functional risk. By identifying high, medium, and low-risk failure modes through historical data, expert opinions, and real-world feedback, test efforts can be focused on the most critical areas. This risk-based method improves diagnostic alignment with real-world failures, simplifies test development, and enhances communication across different teams. It also supports optimization by justifying the reduction or elimination of redundant test points. The paper presents a balanced and scalable methodology for improving test coverage, enabling efficient, risk-aware system-level testing.

Chapter 4

Methodology

This study aims to explore how key principles of the circular economy can be effectively integrated into the PCBA testing process from an electronic design standpoint. The study assesses how testing practices influence sustainability while balancing environmental impact with functional and economic requirements.

4.1 Development Process

In the initial phase of the thesis, a survey was conducted among PCBA and DFT engineers to collect domain-specific insights. The existing testing methodologies, the tools employed in PCBA testing, and the various types of test fixtures in use were systematically analyzed. The findings from this analysis served as the basis for formulating hypotheses regarding potential concepts. The practicality and potential of these concepts to improve sustainability within the production test environment were then evaluated. The research focused on determining the viability of implementing the following methods:

- Modular and reusable test fixture designs for Bed-of-Nails testing
- Alternative testing methods
- Smart relay systems for energy consumption
- Test points optimization

4.1.1 Modular Test Fixture Designs

Test fixtures used in production testing are customized for each specific PCBA (Printed Circuit Board Assembly) and are discarded after use, as it cannot be reused. To address expanding product diversity and accelerated product turnover, the adoption of modular or reconfigurable fixtures is a key enabler. Such fixtures allow for more efficient switching between product variants and significantly reduce the time and resources required for introducing new products. Figure 4.1

shows a Modular test fixture designed by Promoco. For a fixture to be reconfigurable, it must be designed to accommodate an entire product family within a single setup, allowing for quick and efficient reconfiguration to support different variants. Additionally, the fixture should support rapid integration of new products, as product families are dynamic and continuously evolving.

This introduces several critical design considerations, including the frequency of reconfigurations, the time required for each reconfiguration, and the overall effort involved in integrating new products. Another important aspect is the compatibility of these modular fixtures with Electronics Manufacturing Services (EMS). Ideally, the same test fixture should be usable across both production testing and EMS environments to streamline processes and improve consistency. Implementing this concept posed significant challenges, requiring the production testing team and EMS providers to adopt a standardized design.

Despite its flexibility and potential for reuse, modular test fixture design is often not encouraged, especially in EMS environments. One primary reason is the higher initial cost and time investment required for designing modular fixtures. In contrast to specialized fixtures, which are designed for specific products and easier to implement quickly, modular fixtures demand careful planning and complex engineering to ensure compatibility and reusability. In high-volume production settings, where speed, reliability, and consistency are critical, dedicated fixtures are preferred because they minimize test cycle time and are optimized for efficiency. Moreover, modular fixtures can be more prone to mechanical wear and tear due to the use of interchangeable components, and troubleshooting becomes more difficult when failures occur.

Another significant challenge is that modular test fixtures are often not handled properly in EMS environments. Operators typically focus only on basic functionality checks and may not fully understand or utilize the modular aspects of the fixture. This lack of proper training and awareness means that the intended benefits of modularity are not realized. Furthermore, design changes in the product can render parts of the modular fixture incompatible if not updated systematically, which adds to the complexity and cost. Since many operators are not technically educated about fixture design or design updates, there is a gap between the design intent and actual usage on the production floor. As the company prefers simpler, dedicated fixtures that are easier to manage and deploy in fast-paced manufacturing environments, the modular design was deemed unfeasible, prompting us to explore alternative solutions.

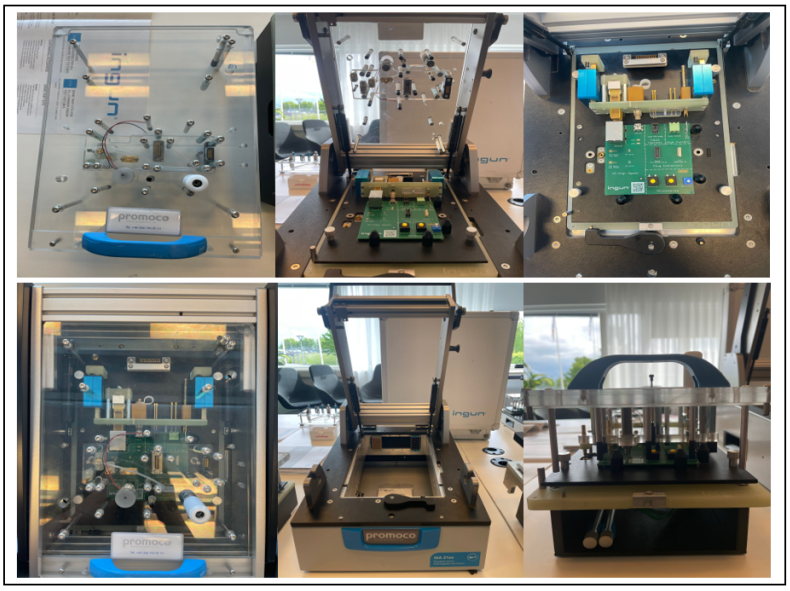


Figure 4.1: Modular Test Fixture designed by Promoco

4.1.2 Alternative Testing Methods-To Reduce The Count of Test Points

The methodology for evaluating alternative test methods focused on two non-fixture-based techniques: Boundary Scan Testing and Flying Probe Testing (FPT). These methods were selected because they eliminate the need for customized mechanical fixtures, thereby reducing setup costs and improving flexibility, particularly during prototyping and low-to-medium volume production.

The first step involved assessing Boundary Scan Testing, which operates by serially shifting data through scan chains via a JTAG interface. Its integration potential with existing Functional Circuit Testing (FCT) was also considered. Boundary scan operations are comparatively slower than standard FCT procedures. In high-volume production environments, this added time negatively impacts test cycle times and overall throughput. Integrating boundary scan requires dedicated hardware (JTAG controllers, probes), software tools, and potentially additional licensing costs. Since many functional failures are already detected through FCT, the inclusion of boundary scan at this stage can be redundant, offering limited return on investment. In some cases, a hybrid approach may be used where boundary scan is partially integrated with FCT. For instance, if the JTAG interface is already being used for firmware programming or if critical components (e.g., BGAs) require structural validation not achievable through FCT alone. However, such integration is the exception rather than the norm and depends on product architecture, test coverage requirements, and production constraints.

The second step involved evaluating Flying Probe Testing, which relies on movable probes that sequentially contact test points. This method was found to

be highly suitable for early validation, troubleshooting, and low-volume manufacturing due to its flexibility and lack of fixture requirements. However, inherent limitations were observed, including slower execution times caused by sequential probe movement, the complexity of trajectory planning on densely populated boards, and reduced capability in performing comprehensive functional and analog tests when compared with Automated Test Equipment (ATE).

While Boundary Scan and Flying Probe Testing offer certain advantages in terms of flexibility and reduced fixture requirements, their drawbacks such as increased test time, additional hardware and licensing costs, and limited suitability for high volume production, make them impractical for integration into Functional Circuit Testing (FCT) within this study. Therefore, these methods were not adopted in the present work and were only considered as alternative approaches during the review of possible test strategies.

4.1.3 Power Optimization Using Smart Relays

In modern production testing environments, optimizing energy usage is a growing concern, particularly when dealing with numerous test stations operating simultaneously. A significant amount of energy is often consumed even during the idle periods of test fixtures, leading to unnecessary power wastage. To address this issue, the implementation of smart relays between the power supply and test stations can be an effective solution. Block diagram for Smart Relay approach is shown in Figure 4.2.

Smart relays are programmable switching devices that can automatically control the power supply to various components based on predefined logic or sensor inputs. By integrating these smart relays into the power distribution architecture of test fixtures, it becomes possible to manage the power flow dynamically. When the test stations are idle or not in use, the smart relay can disconnect the power supply, thereby eliminating standby energy consumption.

This intelligent power management contributes to reduced electricity usage and enhances the overall efficiency of the testing setup. Furthermore, smart relays can be configured to respond to test schedules, operator input, or system status, ensuring that power is only supplied when truly necessary. Over time, this leads to measurable cost savings and prolongs the lifespan of test equipment by reducing continuous exposure to electrical stress.

Integrating smart relays into test fixture setups presents a practical and cost-effective approach to energy conservation. This method aligns well with green engineering practices and supports the development of more sustainable electronic testing environments.

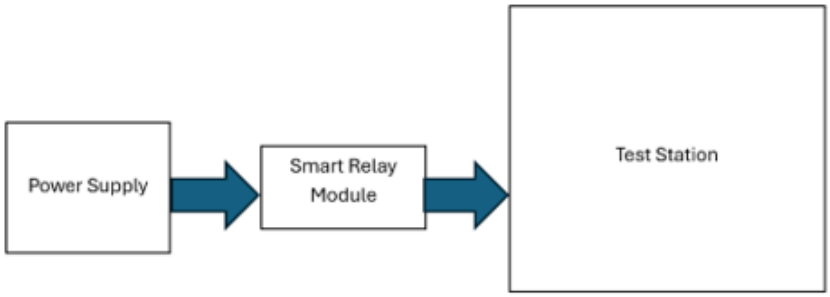


Figure 4.2: Block diagram for Smart Relay approach

4.1.4 Test points optimization

In production testing, the optimization of both the number and placement of test points is crucial for improving test efficiency, cost-effectiveness, and overall reliability. Test points are traditionally added to access key circuit nodes for fault detection and quality assurance during manufacturing. Excessive use of test points can lead to increased PCB complexity, higher fixture costs, and longer test durations often without proportional gains in fault coverage. The position of test points requires consideration of both their functional purpose and their influence on electromagnetic compatibility (EMC) and electromagnetic interference (EMI).Test point positions that are not properly chosen create unintended antenna effects which cause noise interference that disrupts circuit operation and violates regulatory standards [24]. The natural filtering effect of conductor and cable impedances reduces conducted energy at higher frequencies but this effect stops working above 30 MHz. High-frequency conductors and cables transform into antennas which emit radio frequency (RF) energy that disrupts nearby electronic devices [25]. The process of test point optimization involved careful consideration to prevent signal integrity problems and reduce EMI susceptibility particularly in high-speed and analog signal pathways.

To address this issue, Failure Mode and Effects Analysis (FMEA) was used. FMEA is a systematic approach for spotting possible failure types, figuring out how they affect system operation, and prioritizing testing based on risk levels. By integrating FMEA into the test strategy, engineers can focus on high-risk areas, reduce unnecessary test points, and maintain robust fault coverage while optimizing resource usage [26].

Test point optimization helps CAD engineers simplify PCB layout, reduce routing congestion, and improve signal integrity. This reduces the risk of regulatory failures and costly redesigns. Optimized layouts ensure better mechanical access for test fixtures, leading to smoother collaboration with test and manufacturing

teams. It shortens design cycles, enhances product reliability, and supports a more efficient and test-friendly design process.

Classification of Testpoints

The test points are systematically classified into critical, redundant, and optional categories, which helps prioritize testing efforts and make efficient use of time and resources.

Critical test points are the most essential elements of a test plan. These are directly tied to the core functionality, safety, and reliability of the system under test. Any failure in these areas could lead to significant malfunction, security vulnerabilities, or safety hazards. Critical test points usually derive from system specifications, customer requirements, or risk assessments. They include scenarios such as power-on and reset tests, authentication and authorization, or overcurrent and thermal protection in circuits. These tests must be executed without fail, as they confirm that the system performs its intended function under expected and boundary conditions. The successful validation of critical test points is often a prerequisite for system acceptance and release.

Optional test points on the other hand are those that are not mandatory for the core validation of the system but can provide additional insights or improve the quality of the product if time and resources allow. In production testing, these test points typically target non-primary system attributes, including usability characteristics, performance under edge conditions, and exploratory behaviors. Examples include measuring UI responsiveness, verifying functionality under extreme environmental parameters, or observing system response to rare or unexpected inputs. While these tests are not critical for basic functionality, they often help detect issues that may not be captured through standard testing, thus contributing to a more robust and user-friendly system. Optional tests can also be useful for product refinement or competitive benchmarking.

Lastly, redundant test points are tests that do not contribute significant new information to the overall validation effort. These may repeat the same logic, functionality, or data paths already covered by other test points. For example, testing a digital circuit with identical inputs repeatedly, or verifying the same software module with duplicate test cases, are typical instances of redundancy. While redundancy can sometimes help with reliability verification through repetition, excessive redundant test points unnecessarily increase testing time, consume resources, and clutter test reports without improving coverage. Hence, identifying and eliminating such redundant cases is considered good practice.

To implement this classification framework, an in-depth study was carried out for eight different projects. For each project, we obtained and reviewed the main circuit board schematics as well as their corresponding test fixture schematics. This allowed us to understand how test points were chosen initially and distributed across the board. Special attention was given to high-density and high-

risk regions of the circuit where multiple test points were clustered.

In parallel, historical failure data associated with each test point was collected and analyzed using the Qlik Sense application. This data included pass/fail logs from functional circuit testing (FCT) across several production cycles. We tracked how often each test point contributed to identifying a fault and whether it consistently detected the same type of issue. From this analysis, several patterns were identified: some test points frequently captured errors, while others had not flagged any issues over many product runs. Each test point was labelled accordingly using these insights, assigning a critical label to high-value points. All the remaining points were evaluated against the PCBA and test fixture schematics to verify their diagnostic value. The expected behavior of each circuit was analyzed to assess the necessity of the associated test points. Subsequently, the test points were classified based on their functional relevance.

The overall outcome of this approach is a significant reduction in unnecessary test complexity. With fewer redundant and optional test points, test fixtures become less costly to manufacture and maintain. Testing time per unit can also be reduced, which is particularly beneficial in high-volume production. Moreover, focusing on high-risk areas improves diagnostic accuracy and supports quicker root cause analysis when failures do occur. Consequently, this may contribute to greater product reliability and increased customer satisfaction.

Test point optimization using failure-rate-based classification offers a powerful technique for improving test strategy in electronics manufacturing. By integrating quantitative analysis of historical data with in-depth schematic reviews, this study presents a comprehensive approach to intelligent test point management. This method not only minimizes testing costs and time but also aligns with the long-term objectives of quality assurance and ongoing improvement throughout the product development lifecycle.

Chapter 5

Results

This section represents the results of the study conducted. It highlights strategies for improving test efficiency and reliability. Furthermore, this section discusses sustainable practices that can be integrated into the production test environment. These practices aim to minimize environmental impact while maintaining testing performance and quality.The research addressed four key areas; modular and reusable test fixture design, smart relay systems for enhanced power efficiency, alternative testing methodologies, and test point optimization.

5.1 Idle-State Power Consumption Analysis of the Test Stations

In order to quantify the power consumption of the test setup in its idle state, a detailed analysis was conducted. The test station is kept idle for 24 hours and the power consumption was calculated.

Power consumed by Test instruments (PC and Monitor excluded) = 65 W

Power consumed by Test system (PC and monitor included) = 104 W

Power consumed by Test system (PC and monitor included, monitor in sleep mode) = 84W

Let us assume the test station is idle for 24 hours.

Then total energy consumption = 104 x 24 = 2.496 kWh

If it is for 1 month, total Energy = 2.496 x 30 =74.88 kWh

For 1 year, total energy consumption will be 74.88 x 12 = 898.56 kWh

Cost of 1 kWh = 0.89 SEK

Therefore, total cost = 799.71 SEK/year

When comparing the implementation cost of smart relays in test stations to the potential savings in power consumption, it was evident that the latter was significantly lower. As a result, adopting smart relays was not deemed a viable strategy for enhancing sustainability.

5.2 Failure Pattern Analysis in PCBA designs

For test point optimization, the study was conducted across eight distinct projects, each representing different types of surveillance camera systems. These projects included Bullet Camera, Fixed Dome Camera, Multisensor/Multidirectional Quad Head Camera, Multidirectional 4-Channel Camera, Dual Head Camera, Fixed Mini Dome Camera, Panoramic Multisensor Camera and Modular Camera. Each of these projects involves unique PCB architectures, offering a diverse set of test points for analysis. For each project, graphs plotting Yield loss/error rate against individual test points were generated. These graphs provided a clear view of which test points were most strongly associated with the most failures.

5.2.1 Fixed Dome Camera

The main PCBA is composed of several key functional blocks, including the CPU subsystem, power sequencer, Power over Ethernet (PoE) module, IR driver, and audio circuits. Test points vs Yieldloss/Error for this project is shown in Figure 5.1. During the analysis, it was noted that the +12 V ring power section near the audio connector exhibited a higher frequency of failures. This particular issue accounted for approximately 0.50% of the overall yield loss. In addition to the power-related failures, a significant portion of the defects was also attributed to the battery voltage and current loop tests. These areas collectively represent the majority of the observed failure rates, indicating a need for further investigation and potential design or test process improvements in these specific sections of the board. Approximately 22% of the test points have been identified as redundant, indicating potential for optimization. Streamlining these redundant points could reduce fixture complexity by up to 20%, resulting in improved efficiency and potential cost savings in the test setup.

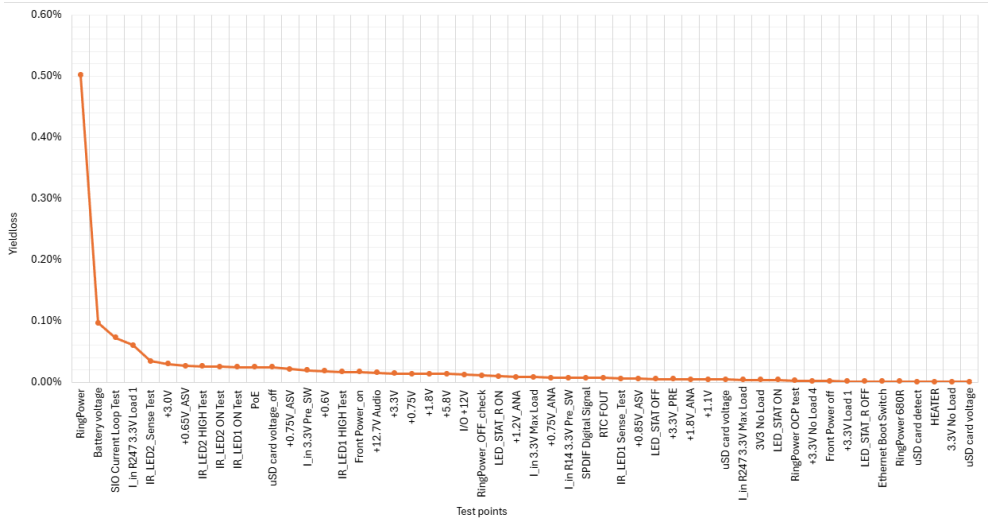


Figure 5.1: Test points vs Yieldloss/Error for Fixed dome camera

5.2.2 Multisensor/multidirectional Camera

The design includes motor drivers to support its functionality. A key observation from the schematics is that a total of 40 test points were defined for the motor drivers, yet only 8 of these were identified as critical for effective testing. The remaining 32 points show limited diagnostic value and can be considered redundant. Figure 5.2 clearly shows that most failures were associated with voltage issues across different nets, rather than motor driver faults. Another important observation is that test points were assigned to temperature sensors, even though their values can be directly accessed through the CPU. This eliminates the need for physical probing in these cases, making the dedicated test points redundant. Overall, approximately 43.9% of the test points are redundant in this project, indicating a significant overlap in coverage. By streamlining the test plan and focusing only on high-value measurements, the number of fixture channels required could potentially be reduced by half, improving both test efficiency and fixture design.

A detailed analysis of a similar project (Multidirectional 4-Channel Camera) revealed that over 47% of the defined test points are redundant, with 43.2% classified as critical for functional verification. This allocation indicates the test plan is excessively weighted toward overlapping measurements. It results in inefficient use of test resources and increased fixture complexity without commensurate gains in fault coverage or diagnostic resolution. Redundant low-value probes should be systematically removed to minimize fixture channel count and reduce test time, thereby optimizing overall test strategy for yield improvement and cost efficiency.

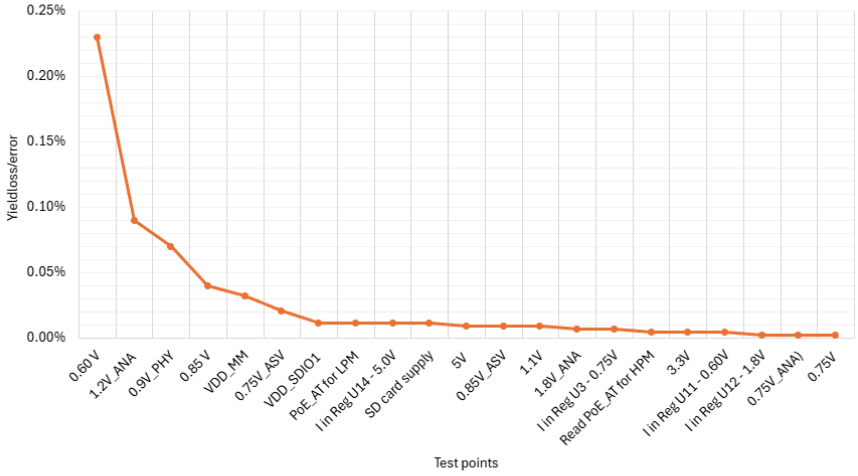


Figure 5.2: Test points vs Yieldloss/Error for Multisensor/multidirectional cameras

5.2.3 Dual-head Camera

Failure data analysis for this project revealed a similar trend. As shown in Figure 5.3, the majority of failures occurred in voltage-related nets and the audio ring power. The main PCBA design incorporates two motor drivers, each originally allocated 10 test points. Analysis determined that only 2 test points per motor driver are required to verify functionality, making the remaining 8 per driver unnecessary. Consequently, 16 motor driver test points were identified as redundant, accounting for roughly one-third of the total redundancy rate.
To improve test efficiency without compromising coverage, it is advisable to reassess these redundant probes and consider reclassifying some as Optional. This approach allows for a more cost-effective and streamlined fixture while maintaining test integrity. Focus should instead be directed toward the 61.9 % of test points identified as critical, particularly those ensuring power and I/O integrity.

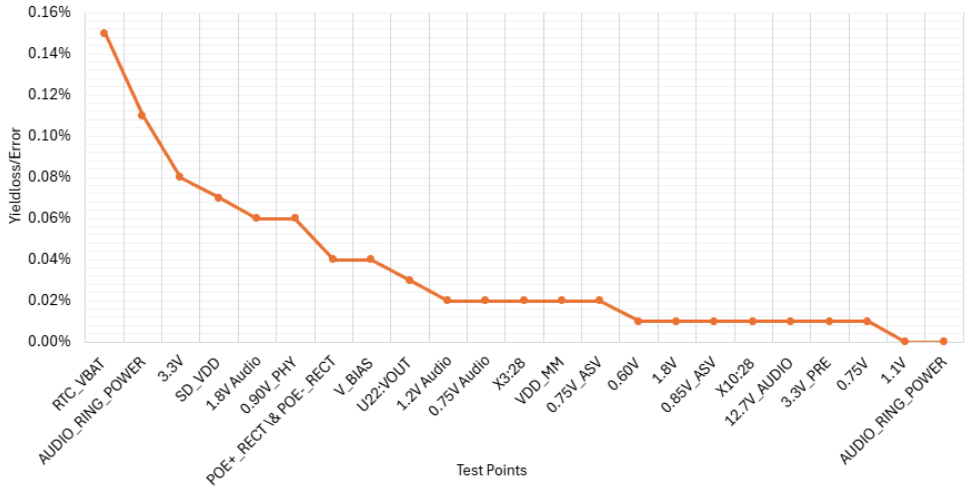


Figure 5.3: Test points vs Yieldloss/Error for Dual-head camera

5.2.4 Panoramic Multisensor Camera

The main PCBA schematics of this project include several key functional blocks: the CPU subsystem, power sequencer, rectifiers, Power over Ethernet (PoE) circuitry, audio codecs, and Day/Night filter drivers. These components form the core of the system's operation and are critical to both power management and signal processing across various modes of the camera.

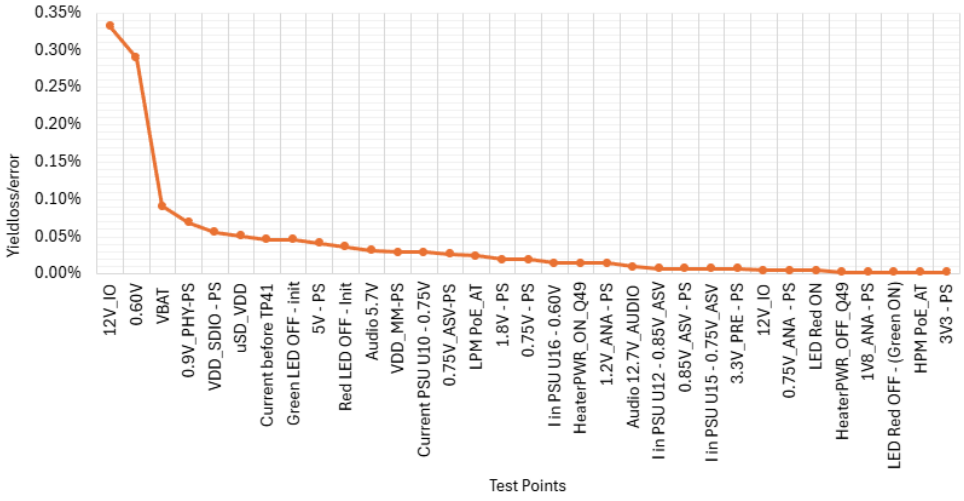


Figure 5.4: Test points vs Yieldloss/Error for Panoramic Multisensor Camera

In this project, a significant portion of redundant test points are associated with the Day/Night filter driver circuitry. Specifically, 8 test points were defined to

verify similar output signals, which introduces unnecessary duplication. Based on functionality, this number can be effectively reduced to just two test points without impacting test coverage. Furthermore, historical failure analysis (Figure 5.4) shows no recorded failures at these points, reinforcing the conclusion that their diagnostic value is minimal. Overall, approximately 33% of the test points in Toothless are classified as redundant.

5.2.5 Modular Camera

The main schematics primarily include the CPU subsystem, ADC converter, power management control, and deserializers. Within the deserializer section, 8 test points were defined. However, these signals can already be monitored through sensors via the CPU, rendering these test points redundant. It is visible from Figure 5.5 that most of the observed failures were linked to voltage evaluation across specific nets, which were accordingly classified as critical for maintaining test coverage and functional reliability.

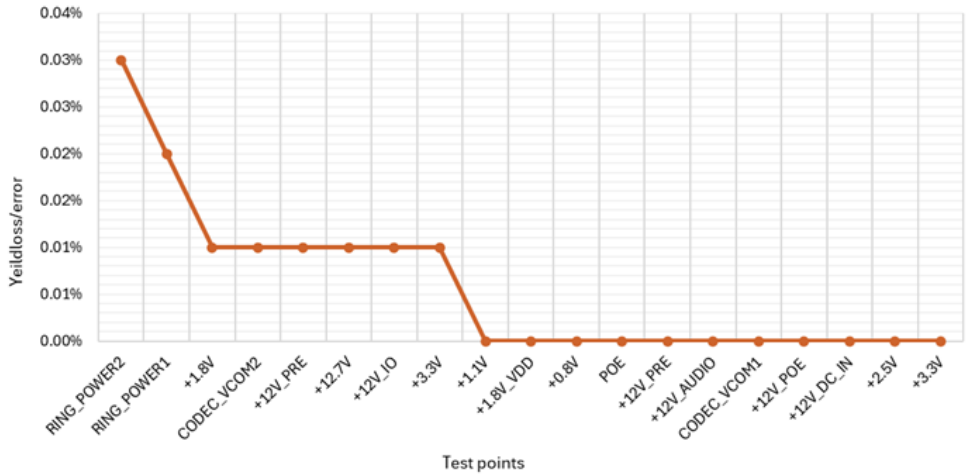


Figure 5.5: Test points vs Yieldloss/Error for modular camera

With approximately 26 % of test points identified as redundant, there is a clear opportunity to streamline the test setup by removing duplicative measurements. While maintaining the current 53% Critical test coverage, it is recommended to reassess the Optional test points. Some of these may be better utilized as lightweight sanity checks rather than requiring full fixture integration, balancing thoroughness with test efficiency.

5.2.6 Fixed Mini-Dome Camera

The main schematics of the fixed mini dome camera PCBA primarily consist of the CPU, power sequencing, SoC power, SoC video, RTC, PoE rectifier, image interface, and PoE switch. Test points vs Yieldloss/Error is shown in Figure 5.6. Analysis of historical failure data revealed that most issues occurred at the VDD_SD test, Supercap test after discharge, and 5V_DN_SUPPLY test points. In this project, a total of 34 test points were analyzed and 44.11% were identified as critical, 29.4% as optional , and 26.47% as redundant.

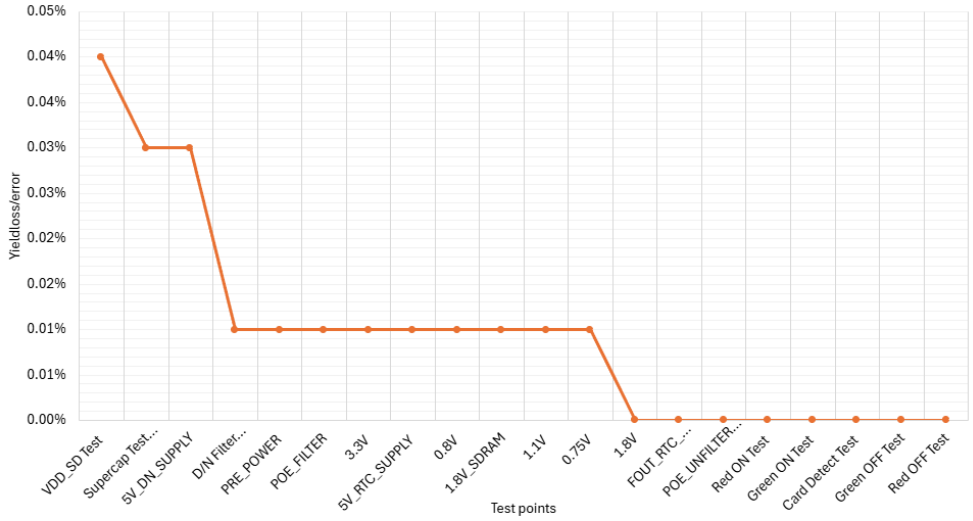


Figure 5.6: Test points vs Yieldloss/Error for fixed mini-dome camera

5.2.7 Bullet Camera

The project involves a compact yet complex PCBA layout designed to accommodate multiple critical components. These include the CPU subsystem, CPU I/O ports and image processing circuits, CPU-LPDDR4 interface, CPU I/O power, power supply sequencer, audio circuits, and network interfaces. This intricate design ensures optimal performance and functionality in a compact form factor.

During the development phase, the main PCBA schematic was meticulously analyzed to identify all test points embedded during the design phase. As shown in Figure 5.7, this analysis revealed that more failures were observed in specific test points, RingPower, VDD_SD ON and TP11 5V3_DC. A total of 49 test points were defined, but failures were observed in only 33 of these test points. 13 testpoints were found to be optional. With over 70% critical coverage and no redundant points, Volley is highly optimized for core functionality testing.

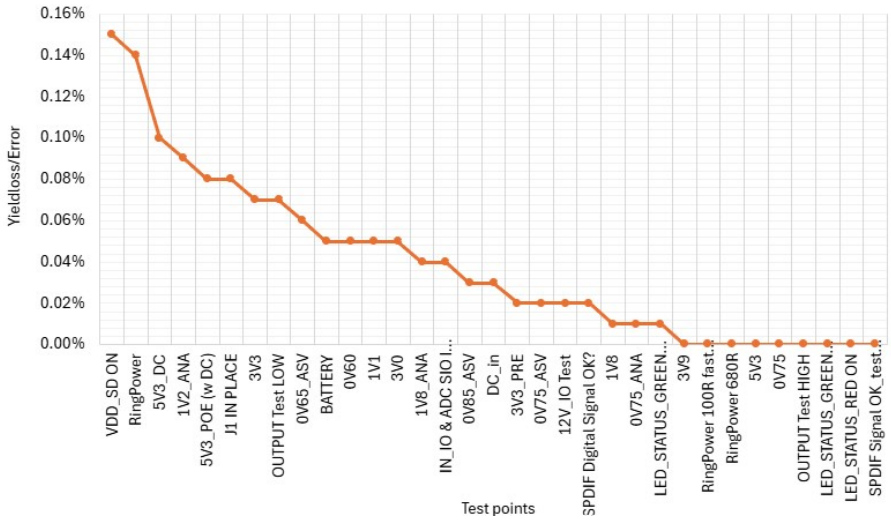
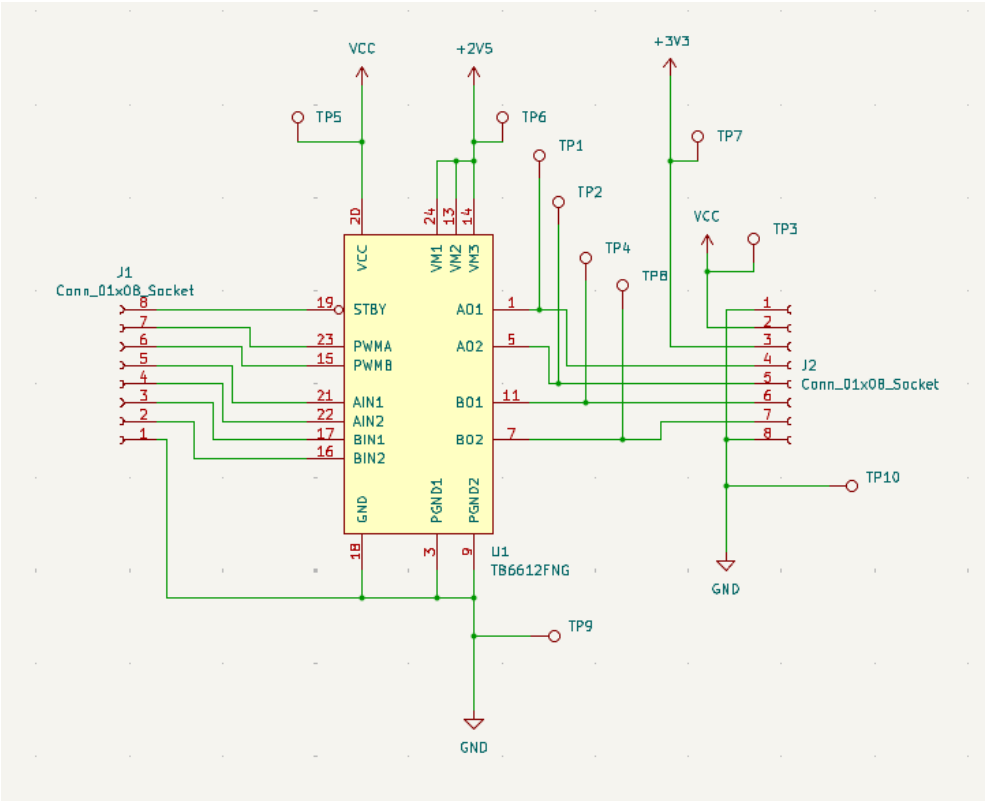


Figure 5.7: Test points vs Yieldloss/Error for Bullet camera

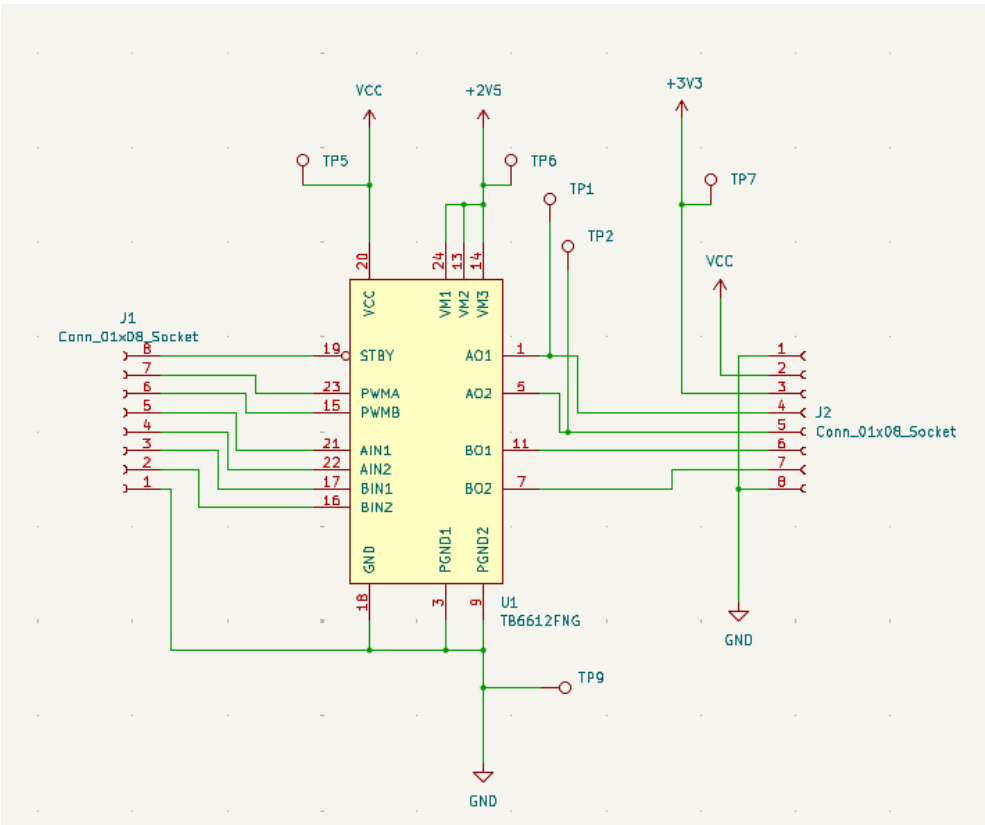
5.3 Proposed Strategies for Test Point Optimization

- The TB6613FTG is a dual H-bridge motor driver IC commonly used for driving DC motors and stepper motors. During the analysis, it was observed that three of the reviewed projects utilize the TB6613FTG IC in its motor driver circuits. In each design, 10 test points were defined per driver to verify functionality. Out of three, two of the projects included four motor drivers each, and the other consisted of two motor drivers, resulting in a total of 60 test points that essentially tested similar functions. These test points were assigned across channels A, B, C, D, and E, without any passive components connected. Consequently, testing each of these points individually leads to redundant effort with minimal added value. Since the behavior across channels is uniform, validating just one representative channel is sufficient to ensure proper functionality. By adopting this approach, we can eliminate approximately 67% of the test points across three projects related to this driver, without compromising the overall test quality.

  For instance, Figure 5.8a illustrates the schematic of a DC motor Driver IC TB6612FNG, designed in KiCad before optimizing test points, highlighting the initial distribution. The chip includes two channels, A and B, each with two output pins, and a test point was assigned to every output for verification. In contrast, Figure 5.8b shows an optimized approach where only one channel is tested instead of both. This reduction does not affect test quality, as the chip's functionality can be validated through a single channel.



(a) Before TP optimization



(b) After TP optimization

Figure 5.8: Schematics of TB6612FNG using KiCad

- The STM32G070RBT6 [27] is a 32-bit microcontroller based on the Arm® Cortex®-M0+ core, operating at up to 64 MHz. It offers 128 KB of Flash, 36 KB of RAM, and a wide range of integrated peripherals, including one 12-bit ADC (2.5 MSps), DAC, UART, SPI, I2C, timers, and USB, making it well-suited for embedded applications requiring efficient and flexible control.

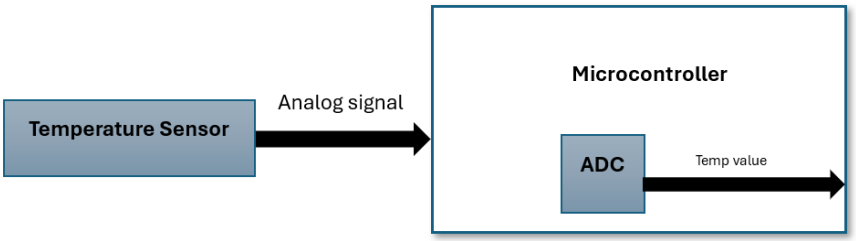


Figure 5.9: Block Diagram for Temperature sensor

It was observed that temperature sensor test points were included in several designs to verify sensor functionality. However, these test points serve limited diagnostic value, as the temperature readings can be directly monitored through the microcontroller's built-in ADC, which is illustrated in the Figure 5.9. The ADC provides sufficient resolution and accuracy to validate the sensor's performance without the need for external probing. The temperature sensor produces a voltage, that changes linearly with temperature. This output is routed directly to the microcontroller's ADC, which converts the analog voltage into a digital temperature reading. As a result, these test points can be safely eliminated, simplifying the design and reducing unnecessary testing overhead, while still maintaining full functional coverage.

- The technique that enables Ethernet cables to carry both information and electric power concurrently is called Power over Ethernet. PoE makes setup easier by removing the requirement for individual power sources, handling typical voltages as high as 48 V, and making it possible to power devices remotely over distances of up to 100 meters utilizing conventional Ethernet cables.
  The test points used to verify functionality can be removed since other methods can be used to check the PoE function. However, keeping some test points separately allows identification of errors or failures at specific points in the system.Another suggestion is instead of using multiple test points for ground, it is better to keep 2–3 common test points to reduce the number of vias for the same function on the PCBA, simplifying the layout and improving reliability.

- DRV8837 [28] is a H-bridge motor driver designed to drive brushed DC motors. It operates from a supply voltage of 1.8 V to 11 V and can deliver up to 1.8 A of continuous current. The device features a simple PWM interface, integrated protection against undervoltage, overcurrent, and overtemperature, and is ideal for battery-powered applications due to its compact size and low power consumption.

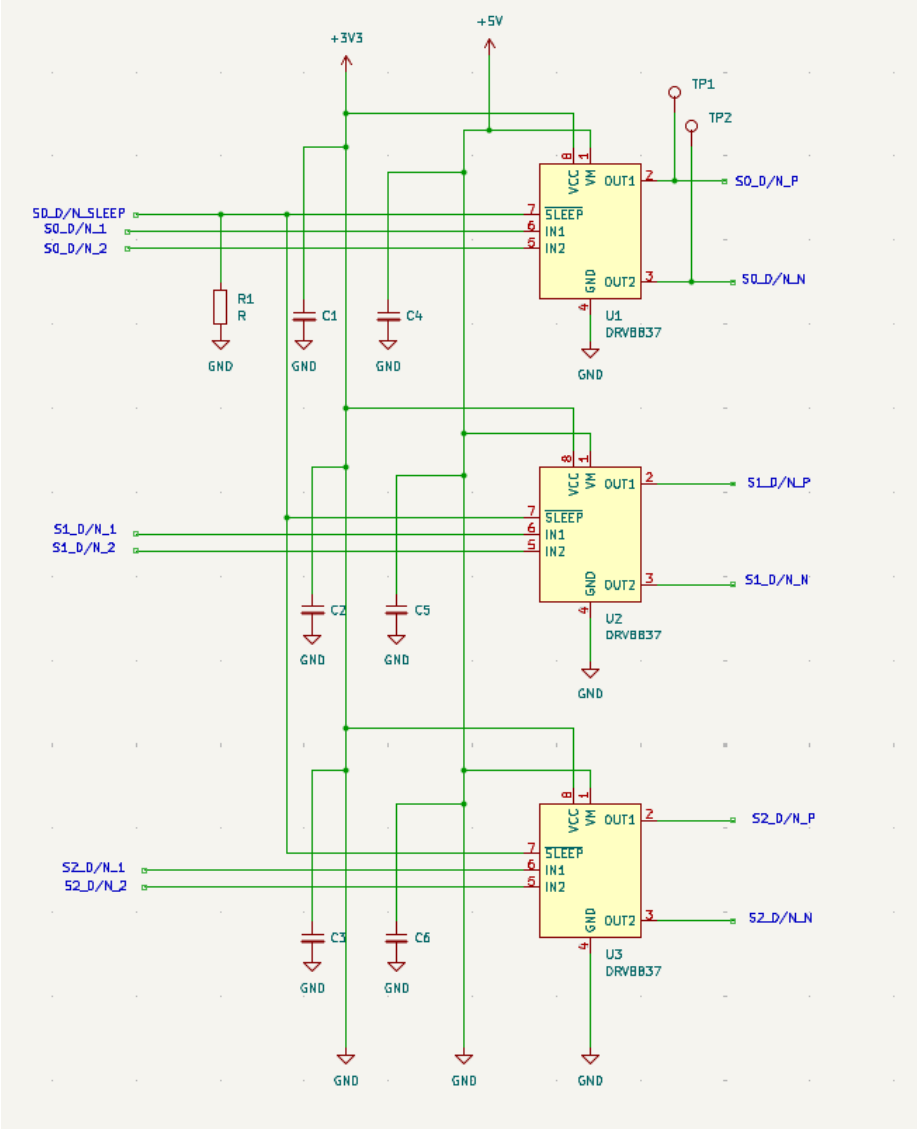


Figure 5.10: Schematics of H-bridge motor drivers after TP optimization

The schematics after test point optimization is shown in Figure 5.10. Instead of checking outputs from multiple test points on the same driver, it is more efficient to test a single output point, as the inputs are interconnected and provide equivalent signals. This reduces unnecessary probing.

5.4 Guidelines for Sustainability in Production Test Environments

1. Test Point Optimization

- Minimizing the number of non-essential test points reduces layout complexity, copper usage, and the potential impact on signal integrity and EMC performance.
- Test coverage should be maintained through intelligent selection of critical test nodes to balance access and minimal design intrusion.
- Where applicable, consider software-based validation or built-in self-test (BIST) to reduce reliance on physical access points.

2. Reusability of Mechanical Components in Customized Test Fixtures

- Certain mechanical components (e.g., fixture frames, alignment pins, probe holders) can be retained after fixture decommissioning.
- Reuse is feasible when parts remain mechanically intact and dimensionally stable.
- Salvaged components can be integrated into new or modified fixtures, reducing lead time and material costs.
- Promotes sustainability by minimizing mechanical waste and resource consumption.

3. Test Time and Resource Optimization

- Parallel testing of multiple DUTs and test step minimization can significantly reduce machine runtime and power draw.
- Use test data analytics to continuously refine test limits and remove redundant test steps that do not contribute to defect detection.

4. Design for Environment (DfE) in Test Planning

- Coordinate with R&D and layout engineers early in the design phase to ensure DfE principles are applied to both the product and its testing strategy.
- Consider life cycle assessments (LCAs) of test equipment to track environmental footprint from manufacture through disposal.

5. Safe Disposal and Recycling

- Maintain a structured protocol for e-waste handling of obsolete fixtures and test boards, including proper sorting and recycling of metals, plastics, and electronics.
- Cooperate with legitimate recycling companies to ensure adherence to RoHS/WEEE directives.

Implementing sustainable practices in PCBA production testing involves a multidisciplinary approach spanning fixture design, electrical testing strategy, energy efficiency, and material management. By adopting modular and reusable fixtures, optimizing test point usage, and reducing power and material waste, manufacturers can significantly reduce their environmental footprint while improving operational efficiency.

Chapter 6

Discussion

The objective of this thesis was to evaluate how circular economy principles, specifically modularity, reusability, resource efficiency and test point optimizations can be integrated into the production test environment for PCBA production testing. The results obtained after studying various projects confirmed that it is technically feasible to reduce material use, fixture complexity, and test time without compromising product quality or fault coverage. However, the effectiveness of the implementation varied depending on the strategy applied.

The study initially explored the feasibility of integrating modular test fixtures into the PCBA production test environment. Although various modular fixtures are commercially available, their adoption is limited due to compatibility challenges with EMS systems, significant upfront costs, and the considerable time investment required for design. Furthermore, modular fixtures are more susceptible to mechanical wear from interchangeable components, and troubleshooting failures is often more complex.

The second approach examined the quantification of idle-state power consumption. However, the potential energy savings were insufficient to justify the implementation costs of smart relays. Consequently, the study shifted the focus to a third approach, investigating alternative test methods to minimize the number of test points. Boundary scan and flying probe testing emerged as possible substitutes for traditional bed-of-nails testing. However, both methods were inherently slower than standard FCT, negatively impacting cycle time and throughput in high-volume production. Additionally, boundary scan integration requires dedicated hardware like JTAG controllers, probes, specialized software tools, and potentially costly licenses.

Finally, the study evaluated test point optimization as an alternative method. Among the various strategies explored, test point optimization based on historical failure rate data proved to be the most impactful and scalable solution in the given scenario. By classifying nets into critical, optional, and redundant,the approach reduced unnecessary probing complexity, lower fixture design overhead,

and improve test cycle time. In several projects, over 30% of test points were identified as low-utility, offering significant opportunity for optimization. These results validate the hypothesis presented in the thesis, that data-driven refinements to test strategy can lead to concrete sustainability gains within existing production frameworks.

This reflection indicates that although not all technical ideas were successfully deployed, the process yielded valuable insights into the constraints and enablers of circular economy implementation in electronics testing. By refining the development workflow and anchoring future solutions in real-world constraints, more sustainable and scalable test strategies can be achieved.

6.1 Societal aspects

This study contributes to the progress of sustainable manufacturing methods, aligning with UN SDG framework, specifically SDG 12.5, which targets a significant reduction in waste production by 2030 through strategies such as prevention, minimization, recycling, and reuse.

From an environmental standpoint, optimizing test strategies and reducing the use of non-essential test points contribute directly to resource efficiency and a reduction in e-waste.The production of electronic devices is naturally demanding on resources, depending heavily on the mining of valuable metals and the utilization of harmful materials. By minimizing unnecessary material use and prolonging the lifecycle of test fixtures, the electronics industry can reduce its environmental footprint. Furthermore, this research has implications for the human dimension of manufacturing operations. Simplified and standardized test systems ease the operational burden on test engineers and production-line operators, particularly in EMS settings where technical expertise may vary. The study also highlights the importance of fostering a collaborative culture between design, manufacturing, and test engineering teams. Such interdisciplinary cooperation is essential for embedding sustainability into product development workflows, ensuring that environmental considerations are integrated from the earliest design stages.

6.2 Future work

Several opportunities exist for extending and building upon the findings of this thesis. The following areas are recommended for future research and development:

1. Integration of Boundary Scan into Functional Test Platforms

Research should be conducted on the co-integration of boundary scan technologies with existing functional test systems. This involves resolving hardware

and software compatibility issues and developing unified test databases and controllers.

2. Impact of Test Point Optimization on Overall Testing Time

Further research may investigate how test point optimization contributes to reductions in overall test time while ensuring adequate fault coverage.

6.3 Conclusions

All test points assigned to the respective projects were thoroughly analyzed. This involved a detailed comparison between the main PCBA schematics and the corresponding test fixtures schematics. Each test point associated with the circuit was examined in detail, including the components used, circuit outputs and test point placement strategy. As part of this analysis, test points were categorized based on historical fault coverage data and their criticality to system functionality. An Excel document was prepared summarizing the findings, covering 483 test points across eight different projects. The insights gathered from this analysis formed the basis for the following conclusions. Across all 8 projects:

- Critical: 261 (54.03%)
- Optional: 76 (15.73%)
- Redundant:146 (30.22%)

This distribution shows that roughly one-third of all test points are redundant, representing substantial opportunity to streamline fixture design and reduce assembly test times. Based on the above result, the following are the interferences.

- Redundancy Is High: Across all eight projects, around 30 % test points were classified as Redundant. This indicates substantial overlap in coverage and unnecessary fixture complexity.
- Critical Coverage Is Under-leveraged: With only 54 % of all test points deemed Critical, there is room to refocus the test strategy on the nets that truly drive device functionality and yield.
- Optional Points as Growth Levers: Optional points (15.73 %) represent a valuable “buffer” where a subset can be elevated to Critical based on risk analysis or historical failures, without incurring the full cost of additional permanent fixtures.

Bibliography

[1] "Sustainable Development Goals." Accessed on 10 August 2025. (2025), [Online]. Available: https://www.un.org/sustainabledevelopment/sustainable-development-goals/.

[2] A. Brent and C. Labuschagne, "Sustainable life cycle management: Indicators to assess the sustainability of engineering projects and technologies," in *2004 IEEE International Engineering Management Conference (IEEE Cat. No.04CH37574)*, vol. 1, Singapore: IEEE, 2004, pp. 99–103, ISBN: 978-0-7803-8519-1. DOI: 10.1109/IEMC.2004.1407084.

[3] G. Mysore, J. Conrad, and B. Newberry, "A Microcontroller-Based Bed-of-Nails Test Fixture to Program and Test Small Printed Circuit Boards," in *Proceedings of the IEEE SoutheastCon 2006*, Memphis, TN: IEEE, 2006, pp. 104–107. DOI: 10.1109/second.2006.1629332.

[4] "Test Fixture." Accessed on 10 August 2025. (2025), [Online]. Available: https://www.promoco.se/en/product-category/test-fixtures/.

[5] I. Pomeranz, "Diagnostic Test Point Insertion and Test Compaction," *IEEE Trans. VLSI Syst.*, vol. 31, no. 2, pp. 276–285, 2023. DOI: 10.1109/TVLSI.2022.3218924.

[6] M. Geuzebroek, J. Van Der Linden, and A. Van De Goor, "Test point insertion for compact test sets," in *Proceedings International Test Conference 2000 (IEEE Cat. No.00CH37159)*, Atlantic City, NJ, USA: Int. Test Conference, 2000, pp. 292–301. DOI: 10.1109/TEST.2000.894217.

[7] "PCB Test Point." Accessed on 20 September 2025. (2024), [Online]. Available: https://www.globalwellpcba.com/what-is-a-pcb-test-point/.

[8] *Test Fixture Signal Interfaces*, FixturFab, 2024. [Online]. Available: https://www.fixturfab.com/articles/test-fixture-signal-interfaces.

[9] "DAQ973A Data Acquisition System." Accessed on 10 August 2025, Keysight. (2021), [Online]. Available: https://www.keysight.com/zz/en/product/34970A/34970a-data-acquisition-control-mainframe-modules.html.

[10] J. Andrews, "IEEE Standard Boundary Scan 1149.1 An Introduction," in *Electro International, 1991*, New York, NY, USA: IEEE, 1991, pp. 522–527. DOI: 10.1109/ELECTR.1991.718268.

[11] *IEEE-1149.1 JTAG and Boundary Scan Tutorial Second Edition*, Asset-intertech, 2022. [Online]. Available: https://www.asset-intertech.com/wp-content/uploads/2022/08/IEEE-1149.1-JTAG-and-Boundary-Scan-Tutorial-Second-Edition.pdf.

[12] "IEEE Standard for Reduced-Pin and Enhanced-Functionality Test Access Port and Boundary-Scan Architecture," *IEEE Std 1149.7-2009*, 2010. DOI: 10.1109/IEEESTD.2010.5412866.

[13] K. P. Parker, *The Boundary-Scan Handbook: Analog and Digital*, 2nd ed. New York, NY, USA: Springer, 1998, ISBN: 978-1-4757-7128-2.

[14] J. Ferguson, "Flying probe test systems: Capabilities for effective testing," in *Proceedings International Test Conference 1998 (IEEE Cat. No.98CH36270)*, Washington, DC, USA: Int. Test Conference, 1998, p. 1163. DOI: 10.1109/TEST.1998.743356.

[15] *Flying Probe Test*, Wevolver, 2023. [Online]. Available: https://www.wevolver.com/article/flying-probe-test-an-extensive-guide-to-the-technology-and-applications.

[16] L. Bonaria, M. Raganato, G. Squillero, and M. S. Reorda, "Test-Plan Optimization for Flying-Probes In-Circuit Testers," in *2019 IEEE International Test Conference in Asia (ITC-Asia)*, Tokyo, Japan: IEEE, 2019, pp. 19–24. DOI: 10.1109/ITC-Asia.2019.00017.

[17] M. Bejlegaard, W. ElMaraghy, T. D. Brunoe, A.-L. Andersen, and K. Nielsen, "Methodology for reconfigurable fixture architecture design," *CIRP Journal of Manufacturing Science and Technology*, vol. 23, pp. 172–186, 2018. DOI: 10.1016/j.cirpj.2018.05.001.

[18] H. V. Tomar, A. Anand, H. L. Harsha, A. Deshwal, and B. N. K, "'Smart Home Automation Device' Using Raspberry Pie and Arduino Uno," in *2022 IEEE 1st International Conference on Data, Decision and Systems (ICDDS)*, Bangalore, India: IEEE, 2022, pp. 01–06. DOI: 10.1109/ICDDS56399.2022.10037544.

[19] J. Moreira, H. Barnes, and G. Hoersch, "Analyzing and addressing the impact of test fixture relays for multi-gigabit ATE I/O characterization applications," in *2007 IEEE International Test Conference*, Santa Clara, CA, USA: IEEE, 2007, pp. 1–10. DOI: 10.1109/TEST.2007.4437582.

[20] Y. Huang, H. Fu, B. Deng, E. Seng, M. Hutner, J.-F. Cote, and G. Eide, "The Advancement of 1149.10," in *2021 IEEE International Test Conference in Asia (ITC-Asia)*, Shanghai, China: IEEE, 2021, pp. 1–1. DOI: 10.1109/ITC-Asia53059.2021.9808741.

[21] M. Portolan, M. Keim, J. Rearick, and H. Ehrenberg, "Refreshing the JTAG Family," in *2023 IEEE 41st VLSI Test Symposium (VTS)*, San Diego, CA, USA: IEEE, 2023, pp. 1–7. DOI: 10.1109/VTS56346.2023.10140015.

[22] "IEEE Standard for Test Access Port and Boundary-Scan Architecture," *IEEE Std 1149.1-2013 (Revision of IEEE Std 1149.1-2001*, 2013, ISBN: 978-0-7381-8263-6. DOI: 10.1109/IEEESTD.2013.6515989.

[23] D. Williams, "Test coverage models for system test," in *Proceedings. International Test Conference*, Baltimore, MD, USA: IEEE, 2002, p. 1185. DOI: 10.1109/TEST.2002.1041893.

[24] P. Chand, B. Gangopadhyay, and M. Kumar, "PCB layout design for EMI/EMC compliance," in *2006 9th International Conference on Electromagnetic Interference and Compatibility (INCEMIC 2006)*, Bangalore, India: IEEE, 2006, pp. 19–24, ISBN: 978-1-4244-5203-3.

[25] X. Luo and J. Tian, "Reducing Electromagnetic Interference in Printed Circuit Board," in *2022 International Conference on Applied Physics and Computing (ICAPC)*, Ottawa, ON, Canada: IEEE, 2022, pp. 314–319. DOI: 10.1109/ICAPC57304.2022.00066.

[26] T. Chen, Yun-shiow Chen, and Yun-Kung Chung, "Implementation of an enhanced FMEA system for the PCBA design testing - a practical case study [failure mode and effects analysis]," in *Proceedings of 2004 International Conference on the Business of Electronic Product Reliability and Liability (IEEE Cat. No.04EX809)*, Shanghai, China: IEEE, 2004, pp. 72–76. DOI: 10.1109/BEPRL.2004.1308152.

[27] *32-bit Microcontroller Unit*, STM32G070RBT6, STMicroelectronics, 2025. [Online]. Available: https://www.st.com/resource/en/datasheet/stm32g070cb.pdf.

[28] *H-Bridge Motor Driver*, DRV8837, Texas Instruments, 2021. [Online]. Available: https://www.ti.com/document-viewer/drv8837/datasheet.

Appendix A

Survey Feedback

To evaluate the real-world challenges and opportunities for sustainability in the electronics production test environment, a qualitative survey was conducted among PCBA test engineers and DFT engineers. The responses highlight a range of technical, operational, and organizational barriers to adopting sustainable practices, particularly in the context of PCBA testing.

A.1 Key Challenges in Implementing Sustainable Practices

Respondents consistently emphasized the constraints imposed by legacy test infrastructure and the lack of flexibility in test equipment. Engineers noted that available test stations and instrumentation must be reused across projects, limiting the ability to implement radically new or sustainable test strategies. Furthermore, product development timelines often prioritize rapid time-to-market, resulting in sustainability being deprioritized in test planning and execution phases.

Geographical disparities in environmental regulations, especially with production carried out at EMS partners in different countries, further complicate the standardization of sustainability efforts. The reuse of PCBA test fixtures remains limited due to product-specific mechanical designs, though partial reuse (e.g., fixture chassis) was considered viable in some cases.

Another significant concern involved data acquisition for power consumption and the implementation of smart energy-saving mechanisms. Engineers cited difficulty in quantifying wasted energy at the station level and integrating advanced solutions like smart relays or idle-state power shutdowns, often due to cost, time, or technical complexity.

Several responses indicated that sustainability is not yet a core focus in the production test domain, with engineers primarily driven by delivery deadlines. Nonetheless, many reported taking individual initiatives such as avoiding redundant orders or attempting to minimize clutter not necessarily for sustainability, but due to workflow optimization.

Additional challenges identified include:

- Lack of structured knowledge about sustainable materials and fixture design.
- Increased costs and labor associated with making reusable fixtures.
- Fragmented ownership and unclear processes regarding fixture end-of-life handling.

A.2 Recommendations for Enhancing Sustainability in Test Areas

Participants suggested several practical strategies to improve sustainability within the test environment:

- Fixture Reuse: Increasing the reuse of mechanical components such as fixture chassis, connectors, and plates by enabling modular designs or maintaining common test point layouts across product generations.
- Shared Infrastructure: Establishing a dedicated team responsible for developing and maintaining generic test fixtures across similar product lines to reduce redundancy.
- Power Management: Implementing automated power-saving mechanisms such as smart relays or shutdown scripts to minimize energy consumption during test station idle periods.
- Material Selection and Recycling: Encouraging the use of eco-friendly and recyclable materials in fixture construction and improving recycling procedures for scrapped components.
- Standardization: Promoting standardization in test architecture and instrumentation to reduce the need for project-specific solutions.
- Fixture Lifecycle Transparency: Improving visibility into the post-delivery lifecycle of fixtures (e.g., tracking reuse, refurbishment, or scrapping in high-volume production).
- Parallel Testing: Exploring parallel testing techniques to reduce test duration and increase equipment efficiency.

A.3 Additional Observations and Ideas

Engineers expressed concern about the volume of waste generated during New Product Introduction (NPI) phases, including scrapped PCBAs and prototype fixtures. Several highlighted the potential for component recovery and reuse in early-stage projects. The need for better knowledge sharing, awareness campaigns, and internal sustainability guidelines was also emphasized.

Ideas for broader impact included:

- Inventory of reusable components: Creating repositories of commonly used connectors or interface modules recovered from scrapped fixtures.
- Second-life equipment use: Reselling or re-purpose obsolete but functional test instruments (e.g., audio interfaces) to avoid unnecessary disposal.
- Data Infrastructure Efficiency: Addressing the environmental impact of cloud-based test data storage, especially high-resolution media and log files, which contribute to energy consumption in data centers.

Overall, the feedback points toward a strong need for cross-functional collaboration, leadership-driven sustainability policies, and long-term planning to align production testing practices with environmental goals.

Table A.1: Historical failure rate of Test points in Fixed Dome Camera

Testpoints	Failed first test	Failed second test	Yieldloss/error
RingPower	1197	1191	0.50%
Battery voltage	230	170	0.10%
SIO Current Loop Test	173	148	0.07%
I_in R247 3.3V Load 1	144	40	0.06%
IR_LED2_Sense Test	82	44	0.03%
+3.0V	71	59	0.03%
+0.65V_ASV	63	45	0.03%
IR_LED2 HIGH Test	61	25	0.03%
IR_LED2 ON Test	60	48	0.03%
IR_LED1 ON Test	58	42	0.02%
PoE	58	24	0.02%
uSD card voltage_off	58	33	0.02%
+0.75V_ASV	51	20	0.02%
I_in 3.3V Pre_SW	46	15	0.02%
+0.6V	43	29	0.02%
IR_LED1 HIGH Test	40	20	0.02%
Front Power_on	40	29	0.02%
+12.7V Audio	36	35	0.02%
+3.3V	34	24	0.01%
+0.75V	32	17	0.01%
+1.8V	32	28	0.01%
+5.8V	32	15	0.01%
I/O +12V	28	23	0.01%
RingPower_OFF_check	26	24	0.01%
LED_STAT_R ON	23	21	0.01%
+1.2V_ANA	19	15	0.01%
I_in 3.3V Max Load	19	2	0.01%
+0.75V_ANA	17	10	0.01%
I_in R14 3.3V Pre_SW	17	9	0.01%
SPDIF Digital Signal	17	14	0.01%

Testpoints	Failed first test	Failed second test	Yieldloss/error
RTC FOUT	17	13	0.01%
IR_LED1 Sense_Test	13	9	0.01%
+0.85V_ASV	13	9	0.01%
LED_STAT OFF	11	10	0.00%
+3.3V_PRE	11	7	0.00%
+1.8V_ANA	10	4	0.00%
+1.1V	10	10	0.00%
uSD card voltage	10	5	0.00%
I_in R247 3.3V Max Load	9	3	0.00%
3V3 No Load	9	6	0.00%
LED_STAT ON	8	8	0.00%
RingPower OCP test	5	1	0.00%
+3.3V No Load	4	2	0.00%
Front Power off	4	4	0.00%
+3.3V Load 1	3	1	0.00%
LED_STAT_R OFF	2	0	0.00%
Ethernet Boot Switch	2	1	0.00%
RingPower 680R	2	0	0.00%
uSD card detect	1	1	0.00%
HEATER	1	1	0.00%
3.3V No Load	1	1	0.00%
uSD card voltage	1	1	0.00%

Table A.2: Historical failure rate of Test points in Multisensor/Mutli-directional Camera

Testpoints	Failed first test	Failed second test	Yieldloss/error
0.60 V	216	135	0.23%
1.2V_ANA	37	37	0.09%
0.9V_PHY	31	31	0.07%
0.85 V	18	18	0.04%
VDD_MM	14	13	0.03%
0.75V_ASV	9	7	0.02%
VDD_SDIO1	5	5	0.01%
PoE_AT for LPM	5	3	0.01%
I in Reg U14-5.0V	5	3	0.01%
SD card supply	5	2	0.01%
5V	4	4	0.01%
0.85V_ASV	4	4	0.01%
1.1V	4	2	0.01%
1.8V_ANA	3	2	0.01%
I in Reg U3 - 0.75V	3	0	0.01%
Read PoE_AT for HPM	2	2	0.00%
3.3V	2	2	0.00%
I in Reg U11 - 0.60V	2	2	0.00%
I in Reg U12 - 1.8V	1	1	0.00%
0.75V_ANA	1	1	0.00%
0.75V	1	1	0.00%

Table A.3: Historical failure rate of Test points in Dual-Head Camera

Testpoints	Failed first test	Failed second test	Yieldloss/error
RTC_VBAT	174	130	0.15%
AUDIO_RING_POWER	131	73	0.11%
3.3V	96	77	0.08%
SD_VDD	76	33	0.07%
1.8V Audio	70	31	0.06%
0.90V_PHY	73	51	0.06%
POE+_RECT & POE-_RECT	51	30	.04%
V_BIAS	45	30	0.04%
U22:VOUT	32	21	0.03%
1.2V Audio	28	19	0.02%
0.75V Audio	23	17	0.02%
X3:28	23	15	0.02%
VDD_MM	23	18	0.02%
0.75V_ASV	28	18	0.02%
0.60V	6	3	0.01%
1.8V	11	7	0.01%
0.85V_ASV	7	6	0.01%
X10:28	16	8	0.01%
12.7V_AUDIO	14	11	0.01%
3.3V_PRE	12	6	0.01%
0.75V	11	6	0.01%
1.1V	4	3	0.00%
AUDIO_RING_POWER	3	3	0.00%

Table A.4: Historical failure rate of Test points in Panoramic Multisensor Camera

Testpoints	Failed first test	Failed second test	Yieldloss/error
12V_IO	135	77	0.33%
0.60V	118	113	0.29%
VBAT	37	27	0.09%
0.9V_PHY-PS	28	24	0.07%
VDD_SDIO - PS	23	16	0.06%
uSD_VDD	21	12	0.05%
I- before TP41	19	15	0.05%
Green LED OFF - init	19	12	0.05%
5V - PS	17	10	0.04%
Red LED OFF - Init	15	9	0.04%
Audio 5.7V	13	8	0.03%
VDD_MM-PS	12	9	0.03%
I- PSU U10 - 0.75V	12	5	0.03%
0.75V_ASV-PS	11	7	0.03%
LPM PoE_AT	10	7	0.02%
1.8V - PS	8	6	0.02%
0.75V - PS	8	7	0.02%
I- PSU U16 - 0.60V	6	4	0.01%
HeaterPWR_ON_Q49	6	2	0.01%
1.2V_ANA - PS	6	4	0.01%
Audio 12.7V_AUDIO	4	4	0.01%
I-PSU U12 - 0.85V_ASV	3	0	0.01%
0.85V_ASV - PS	3	2	0.01%
I-PSU U15 - 0.75V_ASV	3	0	0.01%
3.3V_PRE - PS	3	1	0.01%
12V_IO	2	1	0.00%
0.75V_ANA - PS	2	2	0.00%
LED Red ON	2	2	0.00%
HeaterPWR_OFF_Q49	1	1	0.00%
1V8_ANA - PS	1	0	0.00%
LED Red off- (Green ON)	1	1	0.00%
HPM PoE_AT	1	1	0.00%
3.3V - PS	1	1	0.00%

Table A.5: Historical failure rate of Test points in Modular Camera

Testpoints	Failed first test	Failed second test	Yieldloss/error
RING_POWER2	47	23	0.03%
RING_POWER1	21	16	0.02%
+1.8V	18	18	0.01%
CODEC_VCOM2	10	7	0.01%
+12V_PRE-PreStub	10	9	0.01%
+12.7V_AUDIO	9	7	0.01%
+12V_IO	7	6	0.01%
+3.3V	7	1	0.01%
+1.1V	6	4	0.00%
+1.8V_VDD	4	4	0.00%
+0.8V	3	2	0.%
POE	3	2	0.00%
+12V_PRE	3	1	0.00%
+12V_AUDIO	2	0	0.00%
CODEC_VCOM1	2	2	0.00%
+12V_POE	2	0	0.00%
+12V_DC_IN	2	1	0.00%
+2.5V	1	1	0.00%
+3.3V	1	1	0.00%

Table A.6: Historical failure rate of Test points in Fixed Mini-Dome Camera

Testpoints	Failed first test	Failed second test	Yieldloss/error
VDD_SD Test	403	199	0.04%
Supercap Test after Discharge	263	93	0.03%
5V_DN_SUPPLY	256	134	0.03%
D/N Filter Voltage ON ABS	105	27	0.01%
PRE_POWER	98	60	0.01%
POE_FILTER	98	39	0.01%
3.3V	93	72	0.01%
5V_RTC_SUPPLY	88	25	0.01%
0.8V	74	41	0.01%
1.8V_SDRAM	68	47	0.01%
1.1V	68	18	0.01%
0.75V	51	9	0.01%
1.8V	42	20	0.00%
FOUT_RTC_ Frequency	40	25	0.00%
POE_UNFILTERED	37	14	0.00%
Red ON Test	24	8	0.00%
Green ON Test	17	13	0.00%
Card Detect Test	5	3	0.00%
Green OFF Test	1	0	0.00%
Red OFF Test	1	0	0.00%

Table A.7: Historical failure rate of Test points in Bullet Camera

Testpoints	Failed first test	Failed second test	Yieldloss/error
VDD_SD ON	103	55	0.15%
RingPower	96	66	0.14%
5.3V_DC	64	61	0.1%
1.2V_ANA	62	54	0.09%
5.3V_POE (w DC)	52	50	0.08%
J1 IN PLACE	54	17	0.08%
3.3V	47	38	0.07%
OUTPUT Test LOW	47	29	0.07%
0.65V_ASV	38	38	0.06%
BATTERY	32	26	0.05%
0.60V	36	14	0.05%
1.1V	30	16	0.05%
3V	34	24	0.05%
1.8V_ANA	28	14	0.04%
IN_IO & ADC SIO I loop Test	25	25	0.04%
0.85V_ASV	21	10	0.03%
DC_in	22	20	0.03%
3.3V_PRE	15	12	0.02%
0.75V_ASV	16	9	0.02%
12V_IO Test	11	10	0.02%
SPDIF Digital Signal	14	13	0.02%
1.8V	9	8	0.01%
0.75V_ANA	9	7	0.01%
LED_STATUS_GREEN OFF	6	2	0.01%
3.9V	3	0	0%
RingPower 100R fast OCP test	1	1	0%
RingPower 680R	3	3	0%
5.3V	1	0	0%
0.75V	2	1	0%
OUTPUT Test HIGH	1	1	0%
LED_STATUS_GREEN ON	2	2	0%
LED_STATUS_RED ON	3	3	0%
SPDIF Signal OK_test count	1	1	0%