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Test rig for HMS's platforms

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Abstract

This thesis project was to design, construct, and program a test rig to be used by HMS when checking for faulty connection pins on their testing platforms. The test rig is physically attached to a platform computer at HMS via the pins of the ports on the platform. Our test rig automatically tests the pins of the separate ports in order to analyze and review their parameters and confirm that they are functioning correctly. We developed and designed hardware and software to test two of the five different ports used by the platforms at HMS: the DAQ port and the relay port. Hardware development involved designing couplings, building them, and testing them with preinstalled programs at HMS. The software development involved designing code in LabVIEW that could automatically run tests of the pins of the platform with the help of the couplings we had built. The complete test rig development was successfully completed and proven to work as intended.

Sammanfattning

Detta examensarbete syftade till att designa, konstruera och programmera en testrigg som ska användas av HMS vid kontroll av felaktiga anslutningsstift på deras testplattformar. Testriggen är fysiskt ansluten till en plattformsdator på HMS via stiften på portarna på plattformen. Vår testrigg testar automatiskt stiften på de separata portarna för att analysera och granska deras parametrar och bekräfta att de fungerar korrekt. Vi utvecklade och designade hårdvara och mjukvara för att testa två av de fem olika portarna som används av plattformarna på HMS: DAQ-porten och reläporten. Hårdvaruutveckling innebar att designa kopplingar, bygga dem och testa dem med förinstallerade program hos HMS. Mjukvaruutvecklingen gick ut på att designa kod i LabVIEW som automatiskt kunde köra tester av plattformens stift med hjälp av de kopplingar vi byggt. Den kompletta testriggens utveckling slutfördes framgångsrikt och visade sig fungera som avsett.

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1 Introduction

HMS Networks is a globally recognized company specializing in wireless communication technologies that facilitate information exchange between industrial equipment. The company also manufactures printed circuit boards (PCB) tailored for exclusive and client-specific applications. The process of crafting these different circuit boards involves the integration of a wide variety of components and cutting-edge machinery.

An array of test rigs has been developed to cater to the individual specifications of different PCBs and ensure their optimal functionality when produced. While these test rigs are designed with high precision, a significant problem still occurs. When a PCB registers as faulty during testing, it can be challenging to determine whether the issue lies with the test rig, the PCB, or the platform performing the test. HMS, therefore, initiated this project, which aims to develop a test to check whether the pins of a platform are faulty. The results of the project will make it easier to detect problems and increase testing efficiency.

A platform is a workstation for the employees of HMS and a machine that is used to program and check that different types of PCBs are working. In Figure 1, a typical platform is pictured, and it is from the platform all programmed code and external devices are controlled.

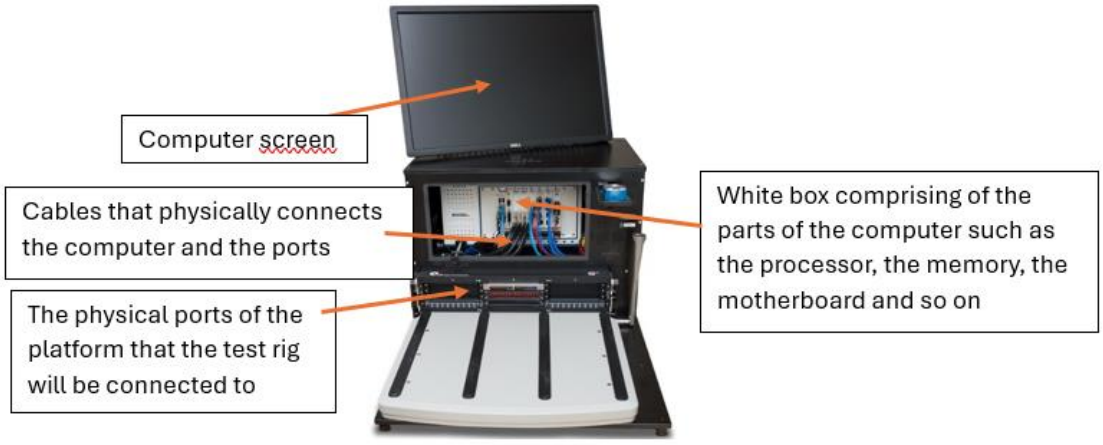

Figure 1 HMS's platform.

The external equipment connected to a platform is called a test rig. In Figure 2, a test rig is physically attached to a platform. The different test rigs redirect various signals from a platform to the right places and connect the platform with external devices that may be needed to check the PCBs for which HMS is responsible. HMS develops many test rigs for checking different PCBs, but they are all mounted to a platform with the same six ports. The platform communicates with the test rig through the channels each port is made up of. The pin is the electrical and physical connection between the platform and the test rig.

Figure 2 Test rig attached to HMS's platform.

The platforms send signals that program and control external devices, and developed test rigs by six physical ports. The ports have different purposes and physical parameters. In Figure 3, the six ports on the platform are shown in more detail. The ports on a platform are connected by physical female connectors, with the test rigs having male physical connectors. The platform controls external devices like National Instrument devices with both the six ports and USB cables.

Figure 3 The six ports on the platform with the position depending on numbers and letters.

1.1 Device specifications

The ports used on the platform that the test rig will be attached to are shown in Figure 3. The table shows the location of the ports in relation to the letters and number positions in Figure 3. The short form name is used regularly in the text to refer to the official name of the port.

Table 1 Port names and locations.

Position	Short form name	Official name	Is it in this project?
A4 & C4	Multi DAQ	X Series PXIe-6345	Yes
B1	VTAC	NI 8234 Dual Gigabit Ethernet Controller, NI PXI-4110 Triple-Output DC Power Supply	No
B3	PSU interface	4 Port Serial Interface, and 2-Port HighSpeed/FD NI-XNET CAN Interface	Used to control other ports
A1	Quadpaddle	PXIe-8430/16	No
B4	Relay card	YAV90132 Relay card	Yes

The ports are made up of different channels depending on the port. In Figure 4, a close-up of the data acquisition (DAQ) port is shown. The figure shows what each channel looks like and where the physical male connector pin is connected.

Figure 4 Close-up on the DAQ port with an arrow pointing towards a channel.

The project aimed to develop a dedicated test rig that can be used to check the integrity of the pins. If a persistent fault is detected in one of the regular test rigs, then the project's rig can be swapped in, and a quick check can be made to see if any pins are faulty. The test rig will considerably reduce the time spent searching for problems by eliminating the need to check all the pins manually.

1.2 Project Overview

HMS tasked us to develop a portable test rig to check their platforms' input and output pins. This was an essential project for HMS that had been deprioritized due to time constraints. Instead, it was constituted as a bachelor's degree project at Halmstad University, with HMS committed to financing the associated costs.

Key specifications included ensuring the test rig was lightweight, easily portable, and robust enough for intensive use. Additionally, it was important for the software aspect to be robust in handling noise and unexpected tests.

Currently, test rigs are moved and mounted on another platform to determine where a potential fault may lie. This involves moving relatively heavy equipment, consumes employee time, and causes disruption in the testing area. Streamlining this process will cause less disruption to employees and enhance operational efficiency.

1.3 Goal

The project's goal was to build and program a test rig to check whether any input and output pins on a platform's ports were faulty and calculate the resistance on every relay in the relay port. HMS's platforms have six ports, but the project's scope was limited to testing the DAQ and Relay ports.

Specifically, the project was to build and develop a test rig that could, by using tests, find out if the input/output channels were faulty. The test rig integrates physical couplings and designed software programs to test the ports used by the platform. The physical couplings had to be compatible with a standard chassis provided by HMS. The software was developed using LabVIEW, the standard platform programming language.

A way to quantitatively determine if the pins on the platform are faulty is essential to ensure that the project results can be verified. The results can be verified by having preset values compared to the measured values, and if they are the same or close to the same within a limit, no fault is present. If the measured value is not close to the preset values, a fault is present, and an idea of what the fault is can be gathered from the result. The results have to account for all known faults and not every conceivable fault. The results must be relatively easy to understand so an HMS engineer can understand them.

The performance requirements include the time needed to complete the tests and the robustness of the designed program to handle unexpected faults or noise that can affect the signals. The disturbance from unwanted noise and resistance must be as insignificant as possible when calculating the resistance of the relays within the relay port. The designed tests must have robust results that are very reliable.

1.4 Limitations

The project aims to integrate the test rig with existing equipment, which imposes strict limitations on flexibility. Zero modifications are allowed to the input/output channels of the platform and the developed test rig because the existing equipment uses them. Any adjustment to channel numbers requires changes in the code and coupling of the test rig and other equipment. Moreover, the test rig is designed solely to establish a physical connection between the platform and itself, without the capability to upload data into circuit boards. The test rig must also maintain practicality, avoiding excessive weight and dimensions. This consideration is crucial for its everyday use and ease of handling by multiple individuals in

the vicinity. Unknown faults will not be considered in this thesis project, as only known faults have results that can be interpreted. Unknown faults will still be touched upon in the report, thanks to error handling.

The platform comprises six ports, but this project focuses only on two. These ports are the DAQ and Relay ports. The ports were chosen because they are the most commonly used at HMS, and due to time constraints, more than two ports could not be selected.

2 Background

2.1 DAQ

There are two DAQ ports, and each includes analog and digital inputs and outputs, several analog and digital grounds, two analog outputs, two analog output grounds, a frequency generator, two analog input sense channels, and two channels carrying +5 V. These channels have different purposes and functionalities, which are described individually below.

If one of these channels becomes faulty, numerous problems could have occurred. The most common is for one of the pins to be broken by an external force. This makes the pin show the wrong voltage, short-circuits the coupling, or not establish a connection at all. These faults are detected by having predefined, acceptable ranges of voltages. If the value is outside this limit, it counts as faulty.

2.1.1 Analog Input Channels

Each DAQ port has 80 analog input channels (AI channels). The analog inputs are used to measure signals from sensors that detect physical quantities such as temperature, flow rate, and pressure. Analog signals in the HMS platforms are built to handle more data than a digital channel. Analog channels are retained as analog signals for as long as possible and are then converted into a digital format by an ADC in the platform. Having the ADC contained in the main chassis of the platform makes it easier to handle noise because optimal shielding can be provided for the ground plane.

2.1.2 Analog Output and Analog Output GND Channels

There are two analog output (AO) channels on each DAQ port, which works like a voltage output. Both channels can deliver a continuous maximum of 5 mA. One channel can deliver 10 V, whereas the other delivers 5 V. There are two analog output GND (AO GND) channels on the DAQ ports, and they are used together with the AO channels to create a differential pair.

2.1.3 Analog GND and Digital GND Channels

There are 11 analog GND and 12 digital GND channels on each DAQ port. Ground channels are used to ensure a safe return path in case of a short circuit and as a reference point for couplings and external devices. The GND channels are designed to handle the same amount of voltage and current as the AI and AO channels. The specifications of the GND channels used by HMS vary according to their purpose [1].

The digital ground is connected to the “digital ground plane, " an area of the platform equipped to handle high-frequency transient voltages. The digital and analog ground are

isolated from each other because of digital noise that occurs in a high-frequency environment of the digital ground [2].

2.1.4 Digital Input/Output/PFI

The digital IO channels use a programmable function interface (PFI) which makes the channels able to switch states between input and output, and vice versa. Therefore, it is necessary to check that each channel works as an input and an output.

The DAQ ports have 24 digital input/output (DIO) channels. The digital input is a pin that measures a voltage and determines if it corresponds to a logic level, classifying it as low or high. These values are then assigned Boolean values of true or false. What a pin input is classified as depends on the standard being used, which in this case is Transistor-Transistor Logic (TTL), which usually ranges from 0.0 to 0.8 V in low and 2.2 to 5.0 V in high. The PFI in DAQ uses the same range but adds 0.25 V to the high threshold.

Digital outputs are the same as digital input, but instead of sensing a voltage, they send a high or low signal [3].

2.2 The Relay Port

The Relay port (called YAV90132) consists of 32 relays that can switch up to 5A. 28 of the 32 relays are single pole double throw (SPDT), meaning the relay has one input and two different outputs.

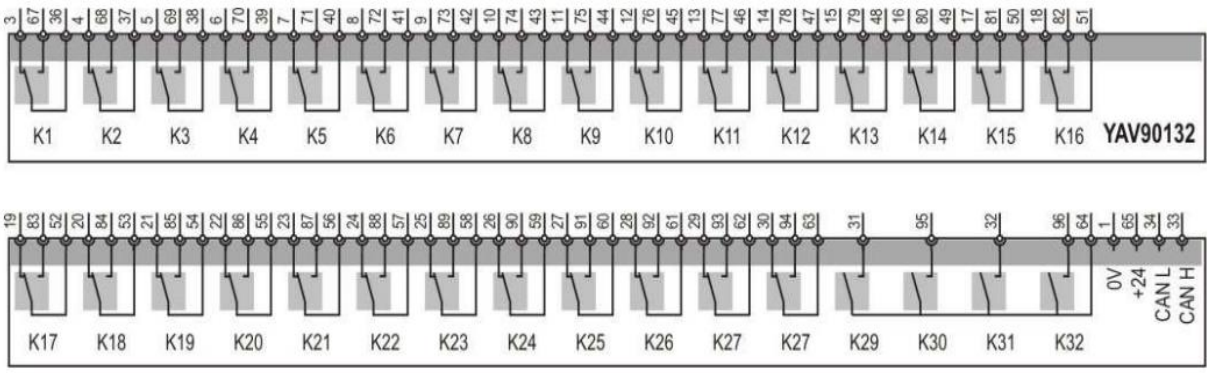

Figure 5 Block diagram for YAV90132. Relay channels signified by K1-K32. In relay channel K1, the input is pin 36, the outputs are pin 3 and 67, and the pole is currently connected to pin 3.

The remaining four relays are single pole single throw (SPST), which means the four relays share a joint input pin, as shown in Figure 5. The pole is the mechanical rod that switches between the outputs. The independent relays are labeled K1 to K27 (there should be a K28 in Figure 5, taken from the HMS documentation [4], but it includes a misprint.) The four relays connected to the joint pin are K29 to K32 [4]. The 28 independent relays have two types, normally open (NO) and normally closed (NC), depending on the test rig wiring. A NO switch is disconnected from the pole by default, and an NC switch is connected by default

[5]. The four relays that are connected to the joint pin are NO. The relays are controlled via a controller area network CAN L and CAN H.

The primary function of an SPDT relay is signal routing in an automatic test system, where it is often essential to ensure that one output is disconnected before another makes a connection. When the pole switches between the outputs, a delay is used to ensure that no interfering signal from the other output is transferred. An interfering signal from the output being disconnected can occur if there is an electric arc from that output.

Stonier and Peter have used SPDT relay switches to optimize solar-powered battery chargers. The SPDT relay's key contribution is to reduce the number of switches and alternate between different battery-charge configurations [5]. Different solar panel configurations such as 4x1 (serial), 1x4 (parallel), and 2x2 (two serial in parallel) could be achieved. As mentioned before, the primary function of an SPDT relay is to perform signal routing. Stonier and Peter use this to change the configuration of the battery chargers when the state of charge reaches a predefined level. Changes in the battery configuration are made to reduce the risk of overheating and overcharging the battery.

2.3 LabVIEW

The coding used by HMS test engineers is performed in LabVIEW. This program utilizes graphical coding instead of the usual text coding. Learning a graphic coding language is considered easier than text-formatted coding, but it still has the same depth. LabVIEW considerably simplifies IO programming and is designed to combine multiple hardware items easily. Additionally, it is designed to make parallel processing as simple as possible. Therefore, LabVIEW is often the choice of companies that test automation and acquisition, processing, and presentation of data [6].

2.4 Other Testing Systems

2.4.1 Contactless I/O Testing

A study made by Stephen K. Sunter, Benoit Nadeau-Dostie, and Logicvision. Inc. used a wafer test to check if I/O pins were faulty. A wafer test is used to get the I/O DC parametric units of the pins. These parametric units are voltage output low (VOL), voltage output high (VOH), current output low (IOL), and current output high (IOH) and are later used to calculate the pin leakage current of each pin. This test includes output voltages and currents, the input voltage, and the pin leakage current. Testing these parameters requires a DC parametric measurement unit (PMU) to be connected to the pins via relay switches. The PMU applies a specific voltage or a current, and the resultant voltage or current is compared to a threshold to determine if the pin passes or fails.
This comparison between the applied signal and the resultant signal is similar to the tests done by the test rig. All analog input pins on the platform are sent a specific input known by

the operator, and once the test is done via the test rig, the operator will see what the pins measured, and if the sent signal is the same as the measured signal, the pin has passed. The analog output pins work similarly, but now, the output from the platform is known, and the test rig measures the input via a PCB [7].

Another practical test is to design a digital IC with a boundary scan and “I/O wrap”. I/O wrap means that the pins are bi-directional. During the IC test, each I/O pad is updated to a logic value, latches the received value, and shifts it out through the boundary scan register. All the pins can be tested in parallel. However, adjacent pins should be driven to different values to permit the detection of pin-to-pin shorts. A leakage current test can be used to test the leakage current of the pins, where each I/O pad is driven to a logic value. When the pin has achieved its logic value, the driver is disabled so that the pad voltage floats and discharges. The pad’s capacitance determines the discharge rate and can later be used to get the leakage current [7]. This IC test is closely related to the test rig’s test of the digital I/Os on the platform. The digital I/O pins of the platform are bi-directional and are tested in parallel by an I/O wrap like the IC test described earlier.

2.4.2 The Overall Design of Multi-state Detection System

Because fixing and troubleshooting circuit boards in the wireless communications equipment area takes time, Wuhan Mechanical Technology College in China [8] has designed a multi-state detection system for wireless communication equipment boards. This specialized environment focuses on key aspects to speed up this problem. Based on the diagnostic strategies of multi-signal flow model optimization design, Wuhan Mechanical Technology College has designed this multi-state detection system, which includes automatic and manual testing. This newly developed system makes detecting, analyzing, processing, and pinpointing faults on standard or special circuit boards quicker.

The design of the Wuhan Mechanical Technology College study addresses the challenges of providing power and controlling signals for wireless communications equipment. These challenges impact the signal detection, extraction, and fault location at the board level. To solve these problems, a subsystem was tailored for wireless communications equipment's internal unit circuit boards. This subsystem is capable of operating in either automatic or manual testing modes. The automatic testing mode generates the various operating voltages and other signals the system needs. It can also analyze and compare the signals the system receives to theoretical or set values to create errors. Using LabVIEW, the software for the automatic testing preprocesses circuit board testing signals, which involves cleaning up the signals and removing noise. After this, relevant parameters, such as the average DC and the RMS, are computed. The RMS calculation is made to calculate the effective level of DC signals. Then, the test results are compared with the standard values stored in the database to determine if they are within the set limit. The software also stores troubleshooting knowledge and test results.

These functions are similar to the test rig project because they both work by generating and receiving signals and comparing them to values already set. This makes it possible to know where the errors are and the reason for them.

The software aspect of Wuhan's study focuses on creating an automatic testing system for circuit boards. It utilizes a multi-signal flow model theory to optimize condition monitoring points and enhance diagnostic reasoning efficiency. The multi-signal flow model theory is a way to describe the processing and interaction of multiple signals within a system simultaneously while also considering their pathways and potential dependencies. This is done to examine how signals flow through a system and to analyze and optimize these pathways [8].

2.4.3 A Universal Life-Test System for Relays

A voltage drop and a current can be used to find the contact resistance of a relay. In the study "A Universal" Life-Test System for Electromechanical Relays" [9], a test of a relay was made, showing information about its contact voltage and current, contact timing, and device operate/release voltage during the test and then showing the parameters graphically for the operator. The study aimed to measure all these parameters during different cycle rates with minimal hardware, and the test design should be simple to understand.

The main idea for calculating the contact resistance for the relay is implemented via the coupling shown in Figure 6.

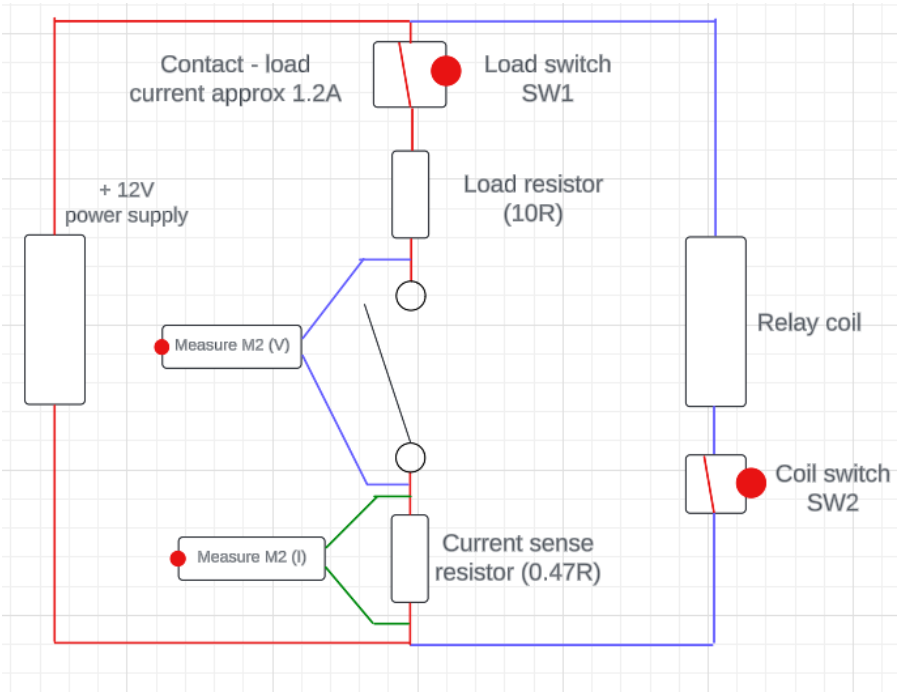

Figure 6 Wiring diagram for relay testing. The blue cables indicate the measurement of the voltage over the relay, and the green cables indicate the measurement of the current going through the relay. The red dot denotes a software-controlled resource.

The relay's voltage is measured during a set amount of time in the programming to calculate the contact resistance. A longer time will increase the result because the time determines the signal quality and stability.

The study uses programming to control the switches SW1 and SW2. The point of using the switches is to control when, for how long, and how often the relay should receive an input. Because of the switches, the relay can be tested, and its value is saved and compared to other saved values. These values are compared, and it is determined what rate is the most efficient. Once the measurements have been made, Ohm's law is used to calculate the resistance in the relay which is saved and compared to future resistance values to determine if the resistance is increasing or decreasing and, in turn, if the relay should be replaced.

This study is closely related to the test rig project because the resistance of the relays is measured and calculated using Ohm's law. This calculation uses both the current flowing through the relay and the voltage over the relay. The difference lies within the programming and some physical structures. One of these differences is that the project will use external devices from National instruments to connect and disconnect the current through the relays and measure the voltage and the current flowing through the relays. The study's programming uses text-based coding language, and the project uses graphical coding. However, the events within the programming will be similar, as a switch will connect the relay, and another switch will allow the current to flow. After that, the voltage will be measured. Once the voltage is known, the switch that controls the current will disconnect, and then the relay will disconnect.

2.4.4 Automated Testing of Electronic Devices

A big part of this study is the software aspect, where an automated test system must be made for the pins and relays on the platform. Dusan Koniar, Libor Hargas, and Marek Paskala have made a study called "Automated Testing of Electronic Devices: Virtual Instrumentation-Based Platform" using action VIs in LabVIEW. This study explains how LabVIEW can test electrical input/output characteristics such as voltages, currents, and frequencies. The study demonstrates that an action VI can be used to set the parameters of physical devices, such as if a pin should be an input or output, how much voltage or current the pin should set, and so on. They also explain that action VIs can be used to both send and read a signal from the physical device and later use that signal to calculate different characteristics.

They say that their automated test sequence consists of 3 main steps: the setup, the main, and the cleanup. The setup section initializes the physical measurement devices and sets what measurements they should take. It also selects the most suitable testing method for the unit. The main part is the actual testing itself, where the action VIs measure and calculate the characteristics of the tested unit. In addition, the main part also determines whether the unit has passed the test by comparing the calculated characteristics to specific set reference points or thresholds. In their study, they store all the measurements in a report file such as PDF,

HTML, or XML. In the last step, the cleanup, all the devices are turned off, and local variables are deleted [10].

A big part of making a test rig for HMS's platform will include action VIs in LabVIEW and learning how to use them. The explanations and examples from Dusan Koniar, Libor Hargas, and Marek Paskala will be used to build further on and fit the goal of the test rig project.

2.4.5 A Hardware-in-the-Loop Simulation Platform for Safety Control Systems

A study to verify safety control systems for nuclear power plants (NPPs) used a unique implementation of data acquisition (DAQ) and hardware-in-the-loop (HIL). Their approach is attractive to the test rig project because it demonstrates how DAQ and HIL can be used to create an efficient and precise platform.

Nuclear power plant safety systems prevent accidents and ensure safe operations. To make sure these systems work before using them in real-life settings, verification and validation (V&V) are used. In their study, a HIL platform was used with DAQ hardware and software to create an environment where the hardware could interact with an NNP simulation.

The DAQ system in their study links the natural and simulated world. The National Instruments (NI) DAQ hardware integrates with a programmable electronics system to synchronize the couplings between the components. LabVIEW is a programmable electronics system and plays a vital role in the DAQ system. It handles signal conversion and routing for signals and provides a user interface for controlling the HIL platform. This combination of hardware and software ensures that the data acquired can be routed and processed correctly.

The HIL platform was applied to test a simplified implementation of the Canadian Deuterium Uranium (CANDU) shutdown system number 1 (SDS1), responsible for monitoring the steam generator level in a simulated NPP. The simulated environment is provided by a Darlington NPP desktop training simulator supplied by Ontario Power Generation (OPG). This simulator offers a realistic representation of an NPP, enabling thorough testing of the safety control system. The simplified SDS1 logic is implemented on an Invensys Tricon v9 programmable logic controller (PLC), a PLC system used in industrial applications. The HIL platform is used to test the performance of both the safety controller and the implemented logic. The platform allows for comprehensive testing by simulating various conditions and theorized initiating events (PIEs), thereby checking the robustness of the safety control system.

This study's insights regarding DAQ, V&V, and HIL usage were significant for the test rig project. It highlighted the need for the DAQ to be able to connect seamlessly to actual hardware and handle signal conversion and routing. Using LabVIEW as the programming language appears to be an excellent choice, given the flexibility and ease of changing the program. Additionally, the capability to manage complex signal processing tasks.

Lastly, the study provided compelling reasons to use DAQ and HIL to test safety control or similar systems. The ability to create a realistic but controlled environment is vital to the test rig project, and it makes V&V a possibility [11].

3 Theory

3.1 Resistance

For the relays in the platform, it is necessary to calculate the contact resistance between the input and output channels. Contact resistance arises due to incomplete connections between the input and output, which build up over time in the relays because of the continuous switching. It is essential to keep track of the resistances between the input and outputs of the relays since they might increase due to three significant factors.

One of the factors are oxidation of the relay contacts. Over time, the contacts might oxidize, increasing the resistance. When a material oxidizes, a layer of oxide occurs on the material and acts as an insulator, decreasing its conductivity and the electron flow.

Moreover, whenever a switch switches between outputs, it hits the contact and causes mechanical wear on the physical contact. This mechanical wear comes from continuous switching operations, and every switch wears down the contact surface. By decreasing the contact surface, the electron flow decreases, and the resistance increases.

An arc light could be created whenever a relay switches due to an electrical current passing through. The high temperature of the light arc could cause the metal to vaporize and react with the air around it, oxidizing the material and increasing the resistance.

Furthermore, when calculating the resistance in a relay switch using Ohm's law, it is of interest to keep in mind that the cables to and from the relay also have resistance depending on the length of the cables, the resistivity of the material, and the cross-sectional area of the cable as explained in Equation 1.

Equation 1 Formula of resistance in cable, where R is the resistance, ρ is the material's resistivity, l is the length of the cable, and A is the cross-sectional area of the cable.

$$R = \rho \frac{l}{A} \tag{1}$$

Due to this, the length of the cables should be as short as possible. Moreover, suppose there are cables between different relays that send identical signals. In that case, it is essential that they are of the same length to give the calculation of the resistance an accurate result.

3.2 Noise

White noise in signal processing is an unpredicted unwanted signal that interferes with the wanted signal in a system. White noise is a complex signal that covers all frequencies with equal intensities. The interference between the wanted and unwanted signals could mask and

change the wanted signal so its outcome looks different. There are many kinds of noise, such as thermal, ripple, shot, flicker, and phase noise. The most critical noises for this project are thermal and ripple noise [12], [13].

Thermal noise arises in all resistive components due to the random motions of the charge carriers within the electrical components. As the temperature increases, electrons move more and have more kinetic energy and random variations. This energy within the electrons generates noise voltage and noise current in the material. Since thermal noise has a white noise spectrum, it also has a uniform energy density distribution throughout the entire frequency spectrum with a Gaussian distribution of energy levels around the mean value of the noise [13].

Equation 2 Formula of gaussian distribution where p(x) is the probability, σ is the deviation around the mean value x.

$$p(x) = \frac{1}{\sqrt{2\pi\sigma}} e^{-\frac{x^2}{2\sigma^2}} \tag{2}$$

Equation 3 Formula of calculation of thermal noise where V is the noise in voltage, k is Boltzmann's constant, T is the temperature in Kelvin, R is the resistance, and B is the bandwidth.

$$V = \sqrt{4kTRB} \tag{3}$$

When measuring analog signals, such as the differential analog inputs on the DAQ port in this project, it is essential to remember that noise will interfere with the signals and change their actual values. The thermal noise arising from the cables in the differential analog inputs in the project can be described as Equation 4.

Equation 4 Noise calculation in the cables.

$$V = \sqrt{4kT\rho\frac{l}{A}B} \tag{4}$$

Thermal noise is impossible to eliminate due to the motion of the carriers within the materials. However, according to Equations 3 and 4, it can be decreased by reducing the temperature, resistance, or bandwidth. In practical terms, this would mean using more efficient components and cables to reduce the resistance, which will decrease the temperature. The noise can also be lowered by installing fans to cool down the circuits. The only way to reduce the thermal noise in the test rig project was to reduce the length of the cables, as this was the only variable the group could change. The components of the project could not be changed due to HMS wanting to use already-bought components, and special orders for the project were not preferred. The bandwidth can also not be changed due to all platforms operating on the same bandwidth of 1.7MHz.

Another part of the noise in the project is ripple noise. This noise arises when an AC signal is converted to DC using rectifiers. When the current has been transformed into DC, some residual AC components remain, which can impact the performance of the components that rely on clean and stable DC power. Since all platforms use an AC DC converter, it will cause ripple noise that interferes with the correct signals. Ripple noise can also emerge when rapid changes occur, such as when using high-frequency relays [14], [15].

The ripple noise filtering can be done in many ways, such as using a resistor-capacitor filter, a Rogowski-Coil Current Sensor, or an LC circuit [16], [17], [18].

The resistor-capacitator (RC) ripple filter decreases ripple noise by connecting a resistor and capacitor in series to filter out the noise from the voltage caused by high switching of the interfacing inverter. The resistance and capacitance are decided by Equation 5.

Equation 5 R is the resistance, C is the capacitance, and T_s is the switching time of the inverter.

$$R * C = 0.1T_s \tag{5}$$

Moreover, if there are different types of ripple frequencies, a zero-ripple filter (ZRF) can be used, which consists of a coupled inductor and a half-bridge active power filter (APF). The purpose of merging the coupled inductor and the APF is to reduce high-frequency ripples with the coupled inductor and low-frequency ripples with the APF [16].

The Ragowski coil current sensor is a feedforward ripple-current active filter consisting of a passive and active ripple filter. The passive part of the filter reduces the ripple noise to an intermediate level, and then the active filter suppresses or even cancels the reduced ripple without undue power loss. The active filter senses the ripple current in the passive filter's conductor and creates a replica with inverted polarity to cancel out the current ripple using a Ragowski coil, a four-stage amplifier, and a current injector.

When the ripple current from the passive filter reaches the start of the active filter, it will first reach the Ragowski coil sensor, comprised of a uniform single-layer winding on a nonmagnetic toroidal core. When the current goes through the coil, it will induce a magnetic field with a voltage, which can be calculated according to Equation 6.

Equation 6 V is the induced voltage, μ is the magnetic permeability in a vacuum, N is the number of winding turns, A is the cross-sectional area of the toroid, I_c is the mean path length around the toroid, and dI/dt is the current flowing through the toroid over time.

$$V = \frac{\mu_o N A}{I_c} \frac{dI}{dt} \tag{6}$$

The voltage induced on the winding is proportional to the derivative of the current passing through the toroid, which means that the voltage waveform looks precisely like the waveform of the ripple current. Once the ripple current waveform has been replicated as a voltage waveform, it goes to a four-stage amplifier that performs necessary frequency shapings and

amplifications for ripple-frequency components while rejecting low-frequency components. The four-stage amplifier consists of noninverting current feedback op-amps. These op-amps and passive components, such as resistors and capacitors, achieve the necessary filtering and amplification. The four stages are one gain stage, two high-pass gain stages, and one ripple-frequency integrator. The ripple-frequency integrator works as a differentiator, increasing the gain by 20dB/decade if the frequency is 1 kHz or lower and decreasing the gain by 20dB/decade if the frequency is higher than 1 kHz.

Once the replicated voltage signal has been filtered and amplified, a current injector creates a current with the exact voltage waveform as the four-stage amplifier created but with an inverted polarity. This current will cancel out the ripple current sensed at the input of the Ragowski coil, and the output of the feedforward ripple-current active filter will no longer have any ripple noise [17], [19].

The feedforward ripple-current active filter could be used within the platforms at HMS to reduce the ripple noise created when the platforms convert AC to DC, which is later sent to the different ports.

Lastly, an inductor-capacitator (LC) filter is also an option. In a study by Hyosung Kim and Seung-Ki Sul, an LC filter was created with a cutoff frequency that limits bandwidth and attenuates ripple noise in a pulse width modulation (PWM) inverter. Their study says that the primary purpose of the LC filter is to attenuate voltage ripple noise made by switching operations. It also states that attenuation can be increased by decreasing the cut-off frequency of the filter against the switching frequency of the inverter, according to Equation 7.

Equation 7 Calculation to increase the attenuation. f_{sw} is the switching frequency, and f_{cutoff} is the cut-off frequency.

$$-40 \log \frac{f_{sw}}{f_{cutoff}} \tag{7}$$

The problem with increasing the attenuation by decreasing the cut-off frequency is that the filter cut-off frequency limits the control bandwidth of the inverter system. A high control bandwidth is essential to keep the inverter operating fast and limit the phase delay. Because of this, there is a trade-off between the attenuation effect and the control bandwidth in the LC filter design.

When the cut-off frequency has been decided, two more problems could occur. One problem is voltage oscillations, which means large voltage spikes may arise in the filter's capacitor when the inverter rapidly changes the output. The spike can be damped out using active damping. Active damping generates a damping voltage negatively proportional to the filter capacitor current. The second problem is the large amount of transient currents that flow through the AC terminals of the inverter when inverters suddenly generate a large amount of voltages. The correct ratio between the inductance and capacitance must be found to minimize the transient current.

The cut-off frequency is calculated as Equation 8.

Equation 8 Formula to calculate the cut-off frequency, where f_f is the cut-off frequency, L_f is the inductance, and C_f is the capacitance of the LC filter.

$$f_f = \frac{1}{2\pi\sqrt{L_f C_f}} \tag{8}$$

If the inductance increases, the transient currents decrease because inductors resist current changes, smoothing out rapid fluctuations. However, the output AC voltage on the load current becomes more sensitive due to the decreased capacitance. Moreover, large inductors can increase voltage stress on the inverter switches, and the voltage drop across the inductor can reduce the available output voltage from the inverter, which Equation 9 explains [18].

Equation 9 Formula to calculate the voltage drop over the inductor. V_L is the voltage drop, L is the inductance, and dI/dt is the current flowing through the inductor over time.

$$V_L = L\frac{dI}{dt} \tag{9}$$

Because of this, an LC circuit is also appropriate to decrease the ripple noise within the platforms in the test-rig project, which would give more accurate analog signals.

3.3 Negative Testing

Negative testing and error handling are important means to improve the robustness of a system. Negative testing is when an unexpected error from, for example, invalid input or stressful environments arises. Usually, a failure is the consequence of an error, which is a difference between a computed, observed, or measured value and the correct value. To prepare a system for faults, it is essential to increase its robustness, which is the degree to which the system functions correctly. The most common way to increase a system's robustness is to do defensive programming. Defensive programming is a type of programming that handles security abnormalities and sends out predetermined outputs if certain failures arise. Because of this, the software can continue to run even if an unforeseen error occurs [20].

Unexpected errors in the test rig can emerge if, for example, a fuse has blown inside the platform due to a high current or a short circuit. It can also emerge in software if a VI does not have the correct controls (input) and indicators (output), giving it invalid information to process or if an external PCB is not connected to the test rig via the USB port on the platform.
The test rig project handles negative testing via an "Error in" handler that passes through all VIs in the program. The error handler is an inbuilt handler from LabVIEW that checks several different aspects, such as a VI not being debuggable, a value being NaN or infinity, an object or reference not found, et cetera. If the error handler detects an error, it will write

what the problem is and where the error was detected. The test rig's program can also handle errors via the code made by the group [21].

3.4 General Testing

3.4.1 Isolation and Continuity Test

Keithley Instruments is a company that develops, manufactures, markets and sells data acquisition products and complete systems for high-volume production and assembly testing. To verify that their pins work after they have been mounted on a breadboard, they conduct two tests: isolation and continuity. The isolation test checks the isolation between two adjacent pins and between the pin and the connector shell so no signals can be misdirected. The insulation between the pins and the connector shell is sufficient. The test applies a voltage between two pins in a connector shell and measures the resultant current that flows between them. The resistance between them is compared to a set threshold. If it is below the threshold, the connector is rejected. Typical threshold levels are between 1 MΩ and 1 TΩ. Continuity is measured between pins to ensure the electrical signals will be appropriately transmitted once the connector is installed. This test is also conducted to control the long-term performance of the pins and connectors. The test involves sending a constant high current through the pin and measuring the voltage drop. The high current has two significant advantages. Firstly, a high current ensures the resulting voltage is above the noise floor of the test system. It is necessary to separate the resulting voltage and the noise. The more separate they are, the better the signal-to-noise ratio and accuracy of the continuity test. Second, if the constant current is higher than the rated current for the pin, it also serves as a stress test for the connector. The stress test of a connector is used to verify its performance margin [22].

3.4.2 PCB Functional Testing

The manufacturing company Valley Services Electronics (VSE) conducts several tests for their PCBs, such as an inspection, metal-to-metal shorts, and a PCB functional test. One part of the PCB functional test is designed to test the PCB based on its operating behavior by simulating its purpose based on its specifications. The simulation is conducted via a connection between cables and the board's connectors, and the software will send different signals and currents throughout the PCB. It will detect analog and digital problems, such as signal distortions, timing issues, and incorrect current levels. Their goal for the test is to conclude if the PCB is functioning as expected based on the specifications given by the client [23].

Another manufacturing company that uses a PCB functional test is PCBgogo. PCBgogo explains that the test is a vital part of their control of the PCB as it helps detect faults as missing parts on the PCB and is cost-effective. Their goal for the test is the same as that of VSE, where the test gives the PCB a pass or not if it meets the client's specifications during the simulated operating environment. Just like VSE, PCBgogo also sends different signals

and currents like the operating environment would to the PCB, and during these signals, the PCB is checked if any components receive the wrong voltage or current, which could occur if there is an incorrect component or if components are missing. They also note that too much insulation resistance can cause a voltage or current problem.
In addition, the test also checks the power integrity, where some common power problems are low-frequency noise, excessive jitter, and Power delivery network (PDN) ripple. If the power supply has fluctuations, it can create a low-frequency noise, which can cause signals to decrease and cause errors in data transmission. Excessive jitter is when the timing of signal pulses or other operations deviates from the correct value. This problem can also lead to degrading signals and performance of the PCB. The last major power supply problem is PDN ripple, when the power supply fluctuates or variates from the actual output, which in turn can cause instability and noise, affecting the performance and reliability of the PCB [24].

4 Method

A prototype test rig was constructed and programmed. The programming entailed creating a code in LabVIEW using block schematics according to HMS standards. Given the complexity and precision of the platform, the hardware part required significant time.

The initial prototype incorporated only the DAQ port. Once the DAQ port testing functioned as intended and had been validated through experiments, the project moved on to the relay port. The goal was to have a working product capable of independently checking each channel, ensuring conformity with standard values for voltage, rated current, and resistance.

The planned method of testing that the test rig works is by setting up errors in each unique channel. Errors were set up for all different channel types of the DAQ by removing the physical pin that connected the platform and the test rig. These errors simulate what would happen if a pin were bent and broken. Another test is sending inaccurate or no voltage, which could happen if a fuse blows in the PSU or the external devices' voltage source has a problem.

4.1 Testing

Manual testing was performed to prove that the test rig's hardware functions as intended. Manual testing can be done physically by looking at every pin on the platform or using programs such as NI MAX that enable, disable, and read channel signals combined with a coupling for the channels on the DAQ or the relay port. These programs simplify manual testing because operators can control and read each channel's value more concretely instead of having to guess or deduce if a pin is damaged. From these values, the state of the channel can be concluded.

Faults were simulated by physically disconnecting a wire between the test rig and the platform, purposefully sending the wrong voltage, or enabling and disabling the signal input/output in the program. These errors can occur naturally after excessive use, and it is therefore essential to have the capability to check whether they have occurred.

When the couplings of the DAQ and Relay ports are ready and operational, the engineers from HMS will run code made by the project group instead of manually testing. This will show if the coupling and code can handle all the known errors and explain to the operator what the error is and where it occurred.

4.2 DAQ

In the development of the DAQ ports, manual testing was used to simulate small replica couplings and verify whether they worked. This manual testing consisted of simple wire

connections, which were only enough to test one pin at a time. When this was verified, a coupling was soldered together like the manual testing coupling, but now all the pins could be tested. When the coupling was finished, it was verified again by manually testing every pin to ensure there were no coupling errors, such as cold joints, and that the coupling worked when more than one pin was being tested. External devices were necessary to build the couplings and were used to provide a voltage source and read values.

A program that used the built couplings had to be developed to make testing the DAQ port's different channels automatic. The program's coding performed tests on one channel type at a time to verify everything was working before moving on. The program's code was made to replicate the manual testing but makes all changes automatically, significantly increasing efficiency.

The two external devices, USB 6001 [25] and USB 6501 [26] from National Instruments (NI), read different data values from the DAQ couplings. A reference ground is provided between the DAQ port and the devices to provide a well-defined voltage level for their ground. USB 6001 comprises 12 analog channels, 13 digital channels, and four analog input differential pairs channels. Therefore, it is ideal for DAQ port testing because it can perform three different measurements. The USB 6501 is also used because, instead of various channels, it offers many more digital channels. These digital channels are needed because the analog and digital GNDs are tested using digital channels. Coupling efficiency and less space usage are increased when using the USB 6501 because more channels are used instead of being empty, which would have happened had only the USB 6001 been used.

4.2.1 Measured Noise in Analog Signals

The platform has a bandwidth of 1.7 MHz, and when measurements on analog differential inputs were made manually, a variation in the signal was approximately ± 0.4 % at 5 volts. This deviation comes from white noise in the cables and connections and must be considered when deciding the voltage limit that triggers an error warning. The limits must be slightly above the deviation values and will be set in the programming.

4.2.2 Digital input/output

The hardware and software aspects of the digital input/output (DIO) test development included making a coupling and coding a program for this test. The coupling was developed by creating a wire bridge connecting two pins, one set to input and the other to output. This coupling tests the pins in the pair for either input or output, so switching the pin states is necessary. The coupling is simply two wires connected between the pins to form a wire bridge. This coupling was used because it takes the least space in the test rig. Another way to build this coupling would be to solder the pairs to a circuit board, which would take up unnecessary space in the test rig and is inefficient.

The program was developed to automatically do a series of operations on each DIO channel to determine if the channel functioned as expected based on the result of these operations. The program starts by setting 12 I/O pins as output and 12 I/O pins as input. The pins are set so that each pair includes output and input. The program goes through each iteration of the program for each pair. When the program runs, it checks whether the input pin senses a high from the output pin. The input signal determines if the pair is faulty or not. As illustrated in Figure 7, when the program has the results of the first 12 input pins, it switches the states of the pins and redoes the test. After every iteration of the program, a string is generated, which is either empty or includes the name of the faulty pin and the location of the pin on the DAQ port in case a fault is detected. Figure 7 is a flowchart model of the program used to test digital input/output.

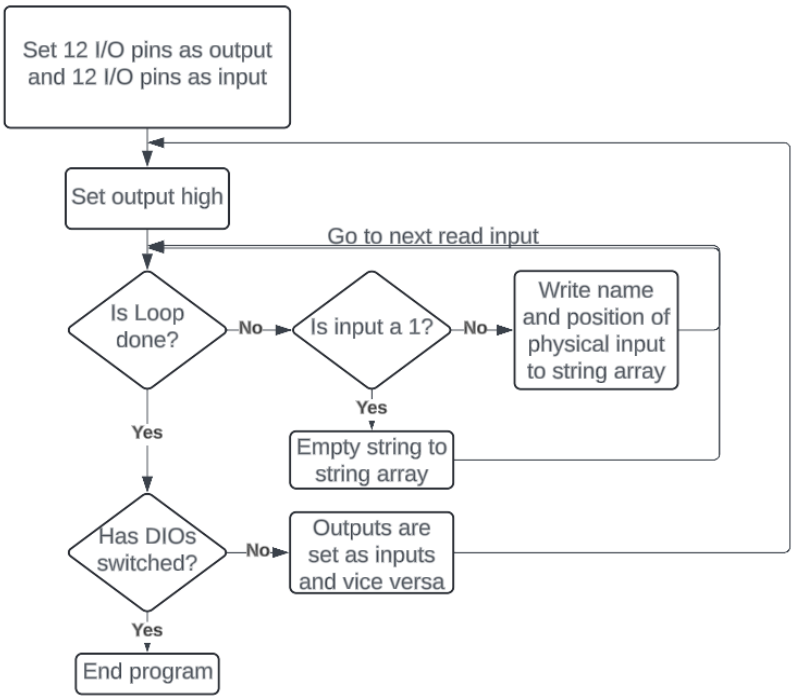

Figure 7 Flowchart of the digital input/output program.

4.2.3 Digital and Analog GND

The physical coupling for digital and analog GND testing uses the external devices USB 6001 and USB 6501 for the first DAQ port, while the second DAQ port only uses USB 6501. The first DAQ port uses both USB 6001 and USB 6501 because, at the start of the development of the digital and analog GND, it was not known that analog GND could be tested with digital signals, and therefore only USB 6001 was needed to test all GND channels. A change to testing both GNDs with digital channels made it impossible to use only one USB 6001 for the lack of digital inputs, and USB 6501 was therefore added. While USB 6501 could have been used to test both digital and analog GND, USB 6001 was still needed for other tests, such as analog output and analog output GND. For the second DAQ port, a second USB 6001 was not required, and a single USB 6501 was chosen to test both digital and analog GND for this port.

The coupling works similarly for both DAQ ports, but the external device used to measure the values differs. The coupling structure is also the same regardless of whether the test is for digital or analog ground. This is because both grounds are tested by digital input channels on the external devices. Figure 8 shows how the finished coupling works. The external device sends 5 V through a resistor, and from there, the voltage can travel two ways: to the digital or analog GND on the DAQ port or back into an input channel on the same external device. A reference point is established by sending a GND signal from the DAQ port to the external devices. The reference GND must be of the same type as the type of GND that is being tested. In DAQ port one, USB 6001 tests the digital GNDs, and the reference GND to USB 6001 must be a digital GND. USB 6501 could be used alone for the second DAQ port because the reference ground for digital and analog could be soldered together. This created a common ground plane for the two different GNDs.

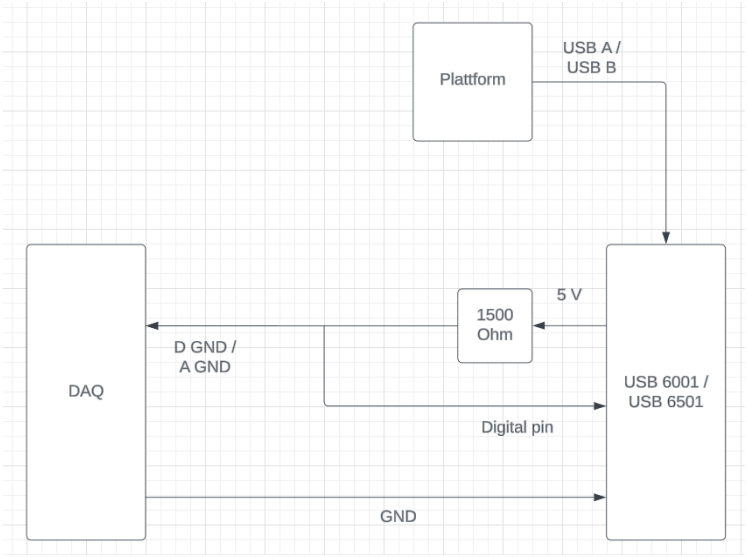

Figure 8 Block schematic of the GND coupling.

The program designed, as shown in Figure 9, for the digital and analog GND activates the input channels on the external device used by that specific DAQ port and reads the input values. The program loops through each input value and checks if they are low or high. If a value is low, it writes an empty string, which signifies that the ground worked correctly. If the value is high, there is a problem with that specific GND, and it writes which of the digital inputs on the external device were used for that iteration. It also writes the position of GND

on the DAQ port. This is because either the GND on the platform or the input channel on the external device is faulty.

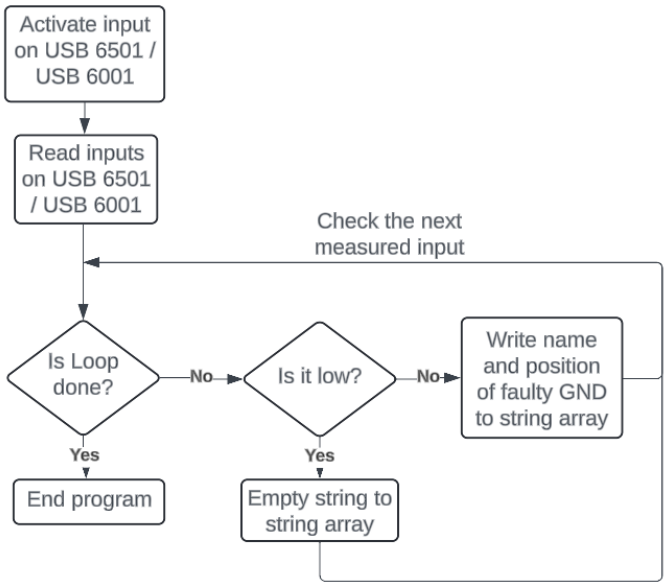

Figure 9 Flowchart of the program for analog and digital GND.

A test that does not test any channel on the ports but is still necessary is the 5 V test. This test tests if the external device's voltage source sends 5 V. This test is required because the digital and analog GND tests use this voltage source for their coupling. The program works as shown in Figure 10, where a digital input channel is activated, and the 5 V are led into this channel. If the input channel state is high, it works. If the state is low, it warns the users of a fault.

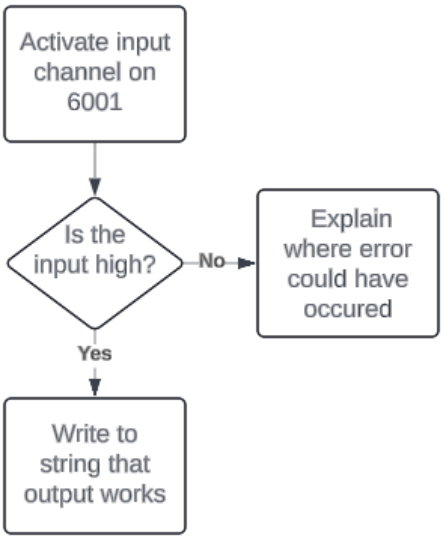

Figure 10 Flowchart of the 5 V tester.

The change to testing digital and analog GND with only digital inputs was previously mentioned because the previous coupling had a flaw. Figure 11 demonstrates the design with the flaw. It functioned as a voltage division to split up the voltage to differentiate between the

results of the tests. This coupling works if analog inputs are used instead of digital inputs. However, digital inputs were the better choice because there are fewer analog than digital inputs on the external devices at HMS. The idea was for the platform to send a voltage through a USB A cable to the USB 6001. USB 6001 then sends 5 V to the voltage divider. If the GND is working, there should be 2.5 V in the digital or analog input of the USB 6001. If it is not working, there will be 5 V in the digital or analog input of the USB 6001. If the input pin is not working, the signal will be 0 V to USB 6001. However, if the 5 V power source output on the USB 6001 is faulty, all the input pins will show 0 V. From this, all the possible outcomes are accounted for. This coupling worked with analog inputs because the signal can be classified as 0, 2.5, and 5 V.
Digital inputs can only have two answers: high and low. This created a problem where there were three possible results, but the program could only represent two. It was noted that the programmed LED on the interface was high for both 5 V and 2.5 V, which means that it was high when the GND was faulty and when it was not. The datasheet for USB 6501, which was used for the digital inputs, explained that the USB 6501 will give a logic low when the input voltage is between -0.3 V and 0.8 V and a logic high between 2.0 V and 5.8 V due to its 4.7 kΩ pull-up resistor. Because of this, a voltage divider was no longer suitable, and a change was made.

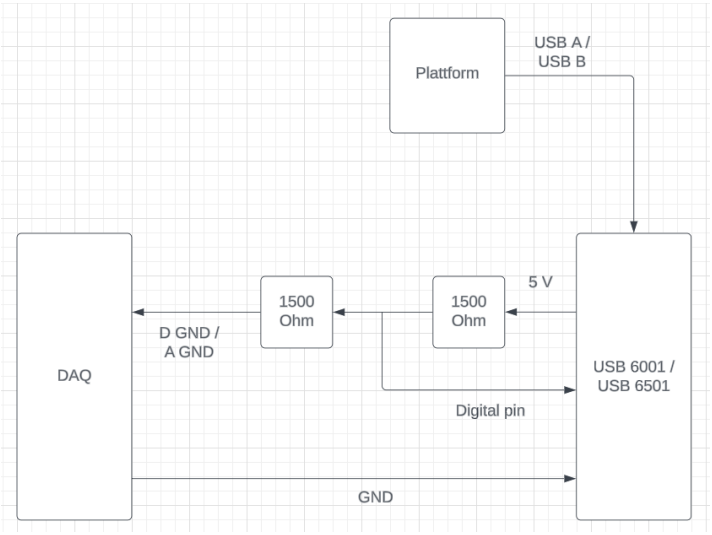

Figure 11 Block schematic of the voltage divider coupling.

4.2.4 Analog output and Analog output GND

The hardware development of the analog output (AO) and analog output ground (AO GND) was to create and design a coupling that tested both the AO and the AO GND. The coupling made for testing these channels is presented in Figure 12. The external device USB 6001 from NI is used to measure the tested channels. The AO and AO GND channels are coupled to a differential pair on the external device. The external device then determines the voltage difference between the signals. The external device sends all the data to the platform through a USB cable. The coupling uses a resistor of 1500 Ω between the DAQ pin and the external

device to decrease the current passing between them, especially if the platform has a fault and sends too much current through the DAQ port.

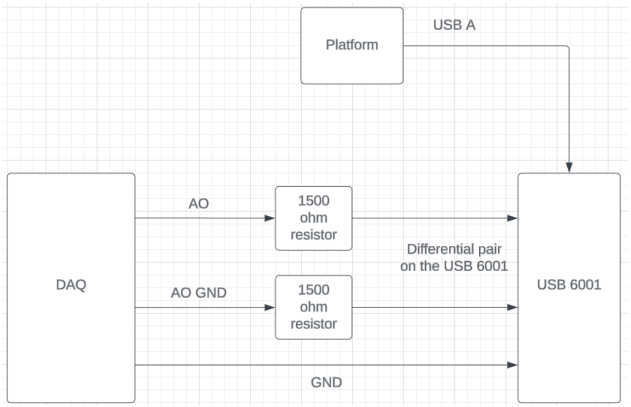

Figure 12 Block schematic of the AO and AO GND hardware coupling.

The program developed to test AO and AO GND with the use of physical coupling is displayed in Figure 12. The program activates the differential inputs on the external device and activates the AO. The program then samples each iteration's AO and AO GND differential. It compares the sampled min and max values to a set upper and lower threshold of 5 ± 0.02 V. 0.02 V is due to the deviation of 0.4 % of analog signals. The range can be easily changed in the software. This is allowed only by HMS engineers to ensure a reasonable range is set. If the analog output were to be changed to 3 V, the range would automatically adjust to 3 ± 0.02 V. Depending on whether the sampled values are inside or outside the threshold, it writes a string of the voltage telling the operators whether it passed the test. When all iterations are complete, the program ends.

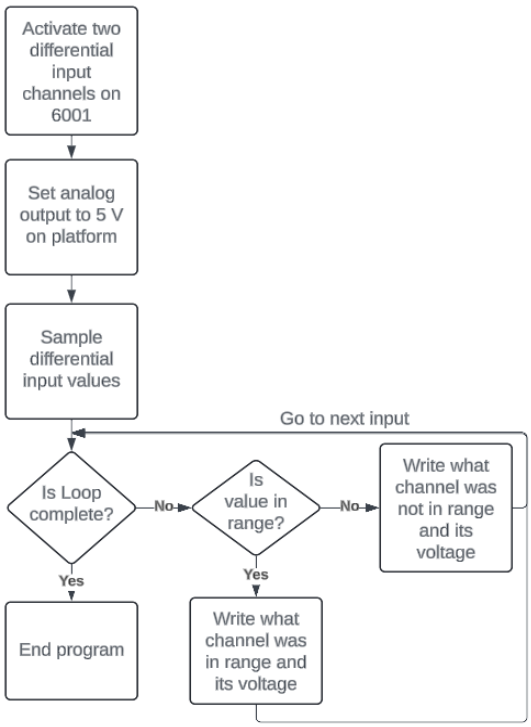

Figure 13 Flowchart of the program for AO and AO GND

4.2.5 Differential Analog Input Pins

The coupling for the differential pins uses the PSU to deliver ± 5 V into all differential pairs of the DAQ port. The PSU channel pair chosen to provide the voltage is constant in this coupling and turns on when a test rig is physically connected to the platform. The coupling structure on all 80 differential pairs from DAQ1 and DAQ2 uses this same PSU channel pair.

Figure 14 Block schematic of the differential hardware coupling.

The program is designed to test each differential pair of the DAQ ports by utilizing the voltage from the PSU. The program starts with doing differential value samples for one second and selecting the min and max of these samples for all 40 pairs. When all pairs' values are recorded, they are compared to a set threshold. This threshold determines if the recorded values are correct or faulty, and a corresponding message will be sent to the operators. If the pair values are correct, an empty string is sent, and if it is deemed faulty, a string containing the voltage and position of the faulty differential pair is sent. The described program is illustrated in Figure 15.

The program had a problem where the voltage of all pins increased or decreased to match the average if they were tested very fast, so if there was only one faulty pin, it was not discernible instantly. This problem was not known until the coding phase because, in manual testing, it takes too long between tests to lead to this problem. This problem is thought to originate from the fact that all differential pins could be connected inside the platform, and rapid testing of the pins causes the other pins to be affected. To solve this problem, a window where the same pin is being tested for one second or more was created, allowing the pin to decrease in voltage if it is faulty. Testing each pin for a longer duration took ten thousand samples at 10 kHz, making for a one-second sample time.

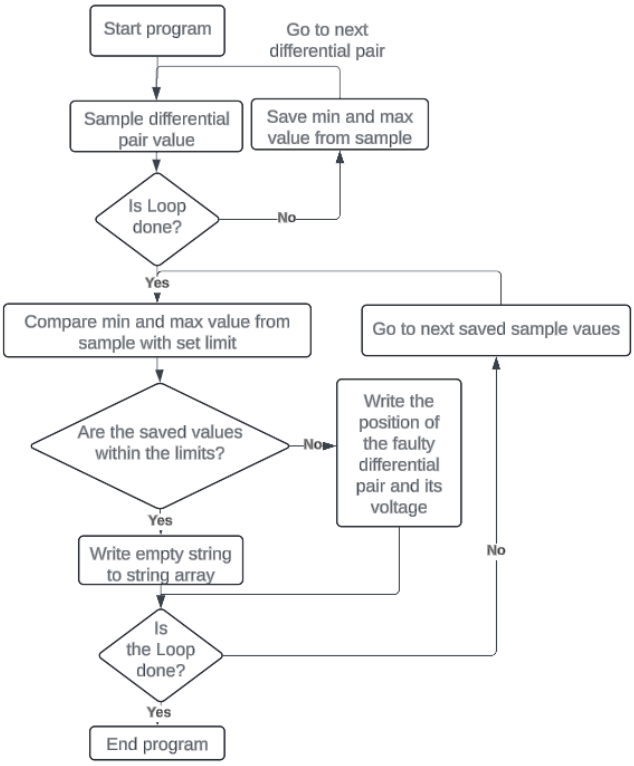

Figure 15 Flowchart of the program for the differential analog input pins.

4.3 Total DAQ

The development of the hardware couplings was performed step-wise and tested separately. This minimized the interference of other couplings and imitated how the programming part was designed to work. When all couplings were ready and confirmed to work through manual testing and the programmed testing system, they were mounted into the test rig. Mounting was done by screwing in two carbon fiber plates that were elevated one centimeter from the bottom of the test rig. The couplings that are made on circuit boards are then screwed into the carbon fiber plate to hold them in place when the test rig is moved. With the circuit boards in place, the wires were zipped together to form groups and fixed in paths that took up the least space. The mounting of the components to the test rig and zipping of cables helped make the space in the test rig better organized, well-structured, and physically robust. Figure 16 shows where the different circuit boards are mounted and what they represent. To the left are the first DAQ port couplings, and to the right are the second DAQ port couplings. The different couplings are color-coordinated to make finding potential errors easier and to identify which group of cables belongs to what test. The analog ground couplings use green cables, and the digital ground uses blue cables. The differential uses yellow and purple cables depending on which DAQ port it is, and digital input/output uses yellow. The 5 V cables are red, and the reference ground for the different external devices is black.

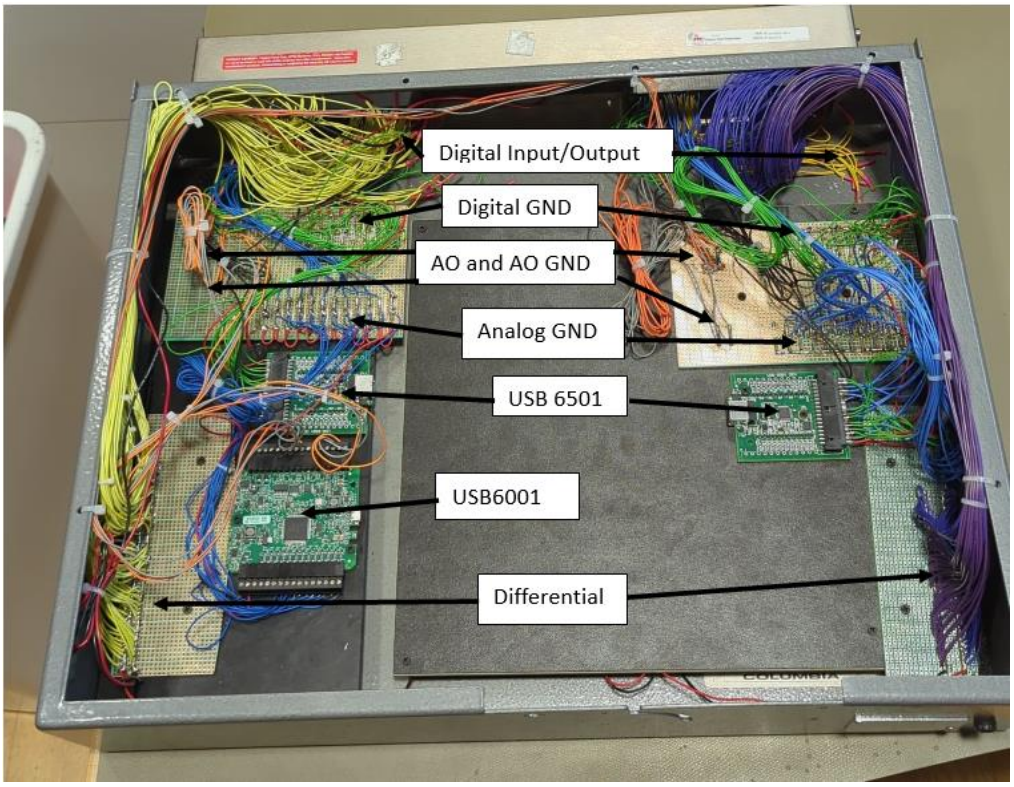

Figure 16 Finished test rig with the hardware couplings for DAQ 1 and DAQ 2.

The program for the VI of the total DAQ uses every test program for the parts of the DAQ. Every programming part of the DAQ has been programmed into a VI with controls (inputs) and indicators (outputs) and put together. In Figure 17, the User Interface (UI) for the total DAQ VI is shown, which includes the 5 V tester, analog GND, digital GND, AO and AO GND, Differential, and digital input/output. In the total DAQ program, it is necessary to transmit an error handler through all test VIs to check for errors. The error handler transmitted through all test VIs is an automatic error handler. It tests if the code works in many aspects, as mentioned in the negative testing segment. If the error handler discovers an error, it will stop all code from running, and this is essential, for example, in the case of a short circuit that could damage the platform. Figure 17 shows the total DAQ UI before the program started. Each square represents where the program will write the results of the test.

Figure 17 UI of the DAQ program.

4.4 The Relay Port

The development of the hardware aspect of the relay port was to design a coupling that could test all 32 relay switches separately and take up as little space as possible. To test all 32 relay switches with the same voltage and current, a coupling that functioned as a closed circuit when no switch was being tested worked best. For this to work, another external relay device was needed to control when and how the different pins in each relay switch pair were connected became apparent. The first thought was a regular relay switch, but this would create too much wear because of the need to switch at least 64 times for each test. The plan was to use a solid-state relay instead to eliminate the problems with using a mechanical relay. The coupling design is illustrated in Figure 18. The figure shows an exact modeling of the coupling except for some skips in relay channels for simplicity's sake. The chosen external solid-state relay is USB 6525 [27], a device from NI. Another external device is USB 6001, which is used as two voltage meters over the relays. These voltage meters are essential to calculate the exact contact resistance over the relays.

The schematic shows how the PSU will send a - 3 V into every relay, which will then travel one of two ways depending on the state of the relay. As shown in Figure 18, the relay outputs will be grouped by the relay's state, bringing every high relay state together, and so forth. The way to test each relay is to set all relays to the opposite state of the one being tested. If the K1 relay's high state is being tested, every other relay is set to low. This makes K1 the only high state and the only way for the current to move through the circuit if the external solid-state relay is controlled correctly. To regulate when the current can pass through the relays, USB 6525 controls when it is a closed circuit.

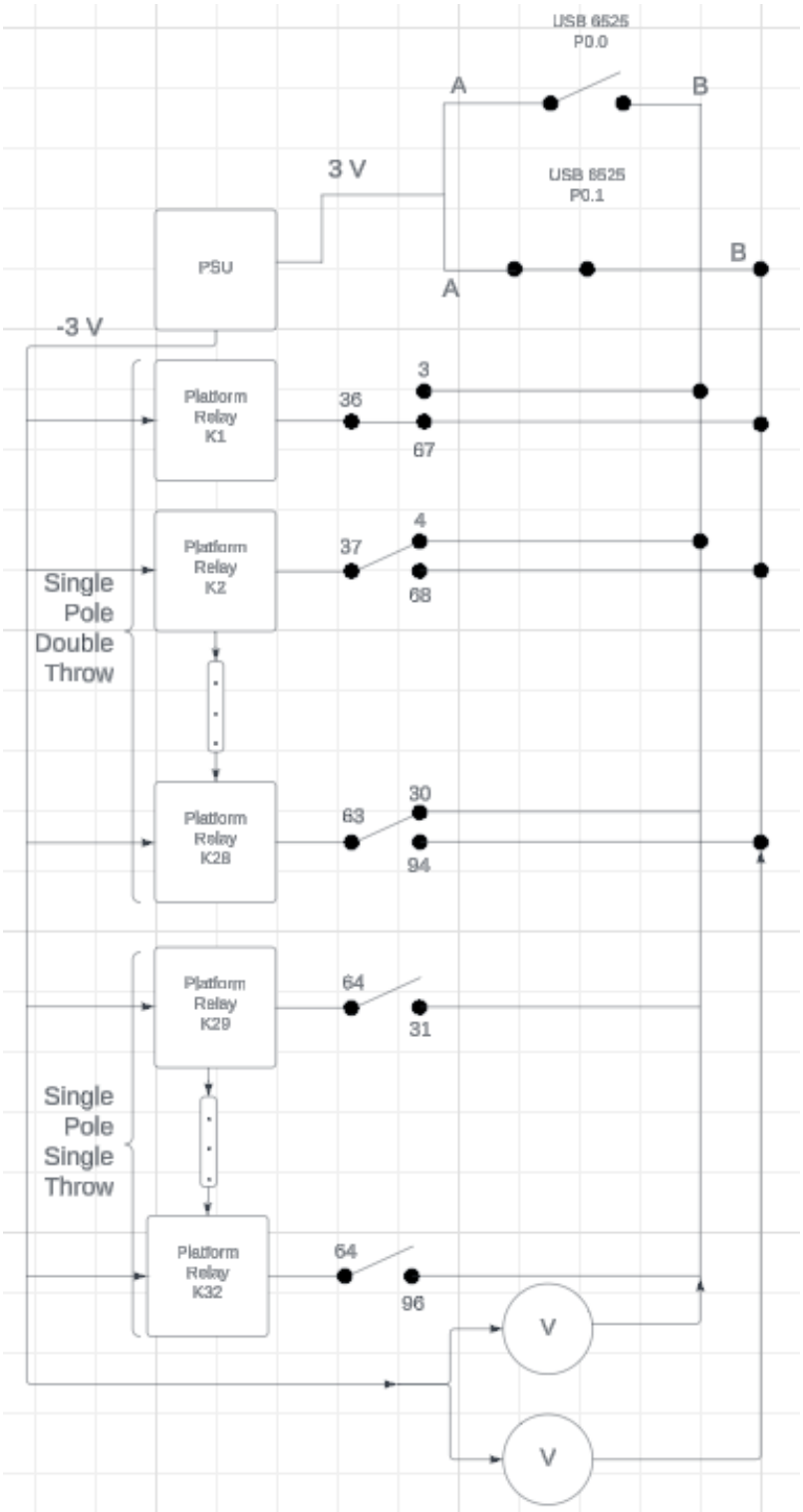

Figure 18 Block schematic of the relay hardware coupling.

Manual testing of this circuit was done using a program named Phi6 to control the states of the relays in the relay port. Additionally, Instrument Studios were used to send a signal of 100 mA with a limit of 3 V. NI MAX was used to control the solid-state relays in USB 6525 and check the voltage in USB 6001. These programs were used to simulate how the coding in LabVIEW was supposed to be designed and check that the designed coupling worked as

intended. The coding started when the manual testing was complete, and the contact resistance values were recorded to compare to the finished product values.

4.4.1 Constant Current to Relay

It was essential to design and find a way to send an almost constant 100 mA and measure this current precisely because the whole program would not work without this. The PSU had an example code that sent a continuous voltage or current and then accurately measured what was sent out. To use this example code, minor changes were made to this example code, which included changing it to only a constant current and a limit on the voltage.

4.4.2 Relay Switching Code

To ensure that the relays were set up correctly and would function as expected at the start of the relay port testing, a code that read the state of every relay was set up at the beginning of the relay port testing program. If the read values were incorrect, it would signify that a relay switch was stuck or broken.

The program was created to set the solid-state relays in USB 6525 to high and low in the correct order. This order changes depending on which state of the relay will get checked. For the first state of the 32 relays, the solid state relay P0.1 is connected, while P0.0 is not connected.

When the relays are in the right state, and the correct solid-state relay in USB 6525 is connected, the program will change the state of every relay separately and measure the voltage during the relay's switched state. This will be done for all 32 relays. After that, the mean for each relay measurement will be divided by the current of 100 mA and multiplied by 1000 to get milliohms instead of ohms, which will be used as the resistance value for that specific contact resistance. A list with all the relay contact resistance values is presented to the operator in the UI. From this list, it can be determined if a value is too high and needs to be changed. Figure 19 shows how the program tests all relay contact resistance.

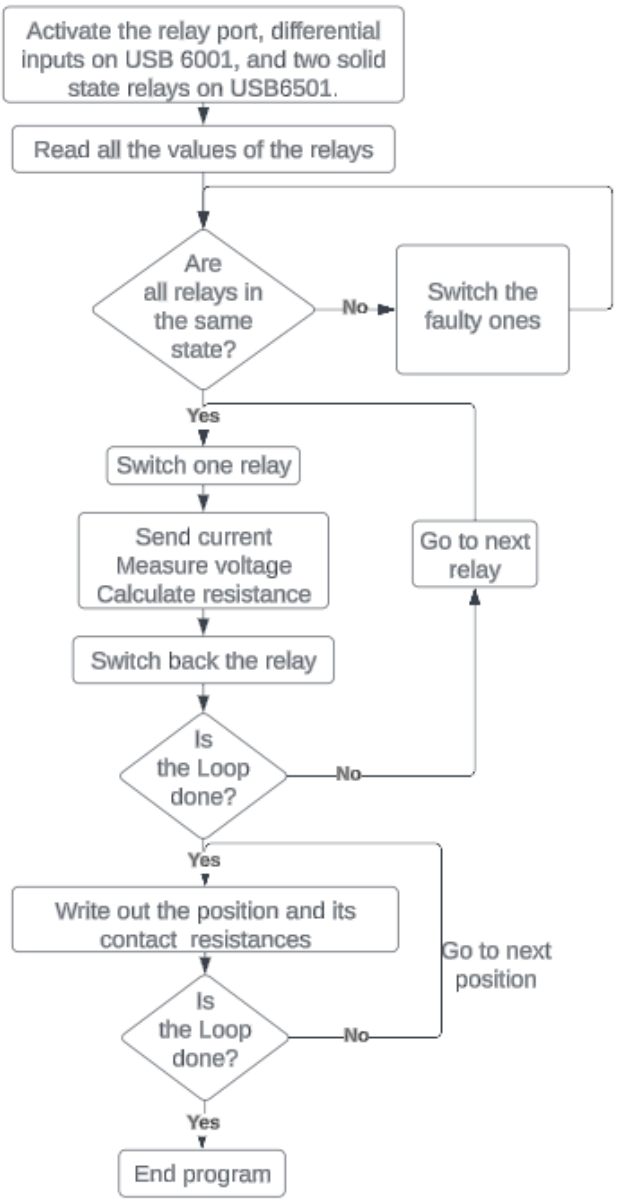

Figure 19 Flowchart of the program for the relay port.

4.5 Total System

Once the hardware and software of DAQ1, DAQ2, and the relay port were completed, everything was put together into a program that checks all the pins and relays within these ports. This program's UI will tell the operators at HMS if any pins are faulty and show the contact resistance of all the relays so that the pins on the DAQs or the relays can be changed if necessary. The three ports were put together to make the results show up on a single UI and be easier to read.

To distinguish the errors between the identical DAQ ports, the UI has text that says which error message belongs to which port. All the text boxes and graphs on the interface are named after what they do and which port they check. The relay port has two boxes for each relay's contact resistances.

The block schematic diagram in Figure 20 shows how each device and built circuit board is connected to control the pins and relays on the ports in the platform and gives an overview of how all the parts are used across the whole project.

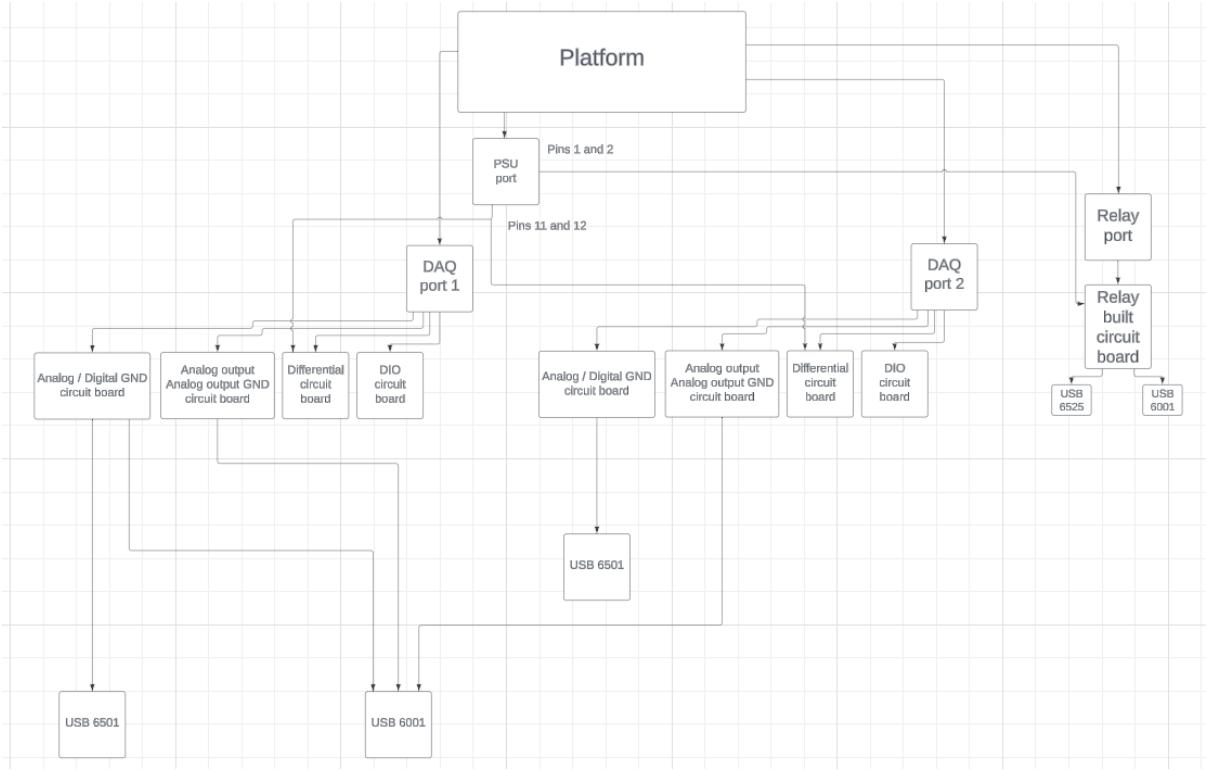

Figure 20 Block schematic over the entire test rig with all components.

5 Implementation

5.1 DAQ

Both the hardware and software for testing the DAQ ports have been completed. All the couplings are soldered together on different circuit boards in the hardware part. Some couplings used external devices to function as sensors. The circuit boards and external devices have been mounted on carbon fiber plates and placed in the test rig, as shown in Figure 16. The report's methodology section discusses how the tests use couplings and how the program for the tests is designed. Manual testing has also been conducted on all pins on the DAQ port to prove that the couplings are correct and function as designed. The manual testing resulted in easier programming because the software only needed to replicate the manual testing and not figure out new procedures different from the manual testing carried out.
In addition, the software part of the DAQ ports testing has also been completed. As explained in the methodology section, every type of pin section has its own programmed VI to check the pins. These VIs are combined into a single program, Figure 21 shows the UI of the combined VIs.

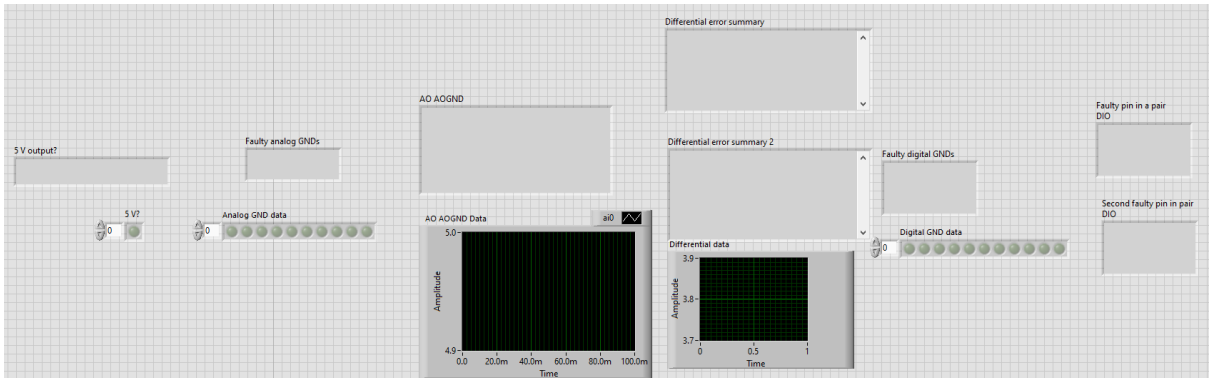

Figure 21 UI of the total DAQ program.

When the test rig searches for errors on the platform, it cycles through all the pins and saves the name and position of any pins found to be faulty. The names and positions of the faulty pins are displayed on the UI once the entire program is finished. Because of this, HMS can quickly locate and fix the faulty pins on the port.

During the project, a switch to another platform created a surprising problem. This platform switch was because the first platform had a slow processor, and the new platform was thought to be faster. A fault occurred when doing a test with a coupling and program that had been verified on the new platform. This new fault was not a simulated error but happened naturally. After some testing, it was proven that this new platform had a faulty channel in one of the ports. This error was not simulated and proved that the verified code and coupling could identify simulated as well as non-simulated errors.

5.2 Relay

The coupling and programming of the relay port are completed. The hardware used different external devices and built couplings with soldered wires connecting the channels mounted onto the test rig. The mounting used screws and nuts to hold every piece still and to keep the hardware robust, as shown in Figure 22. The report's methodology section discusses how the circuit boards and external devices function and are connected. The programming of the relay port has also been completed, and it has been verified to work. Moreover, manual testing was conducted on every relay switch to prove that the coupling and programming worked by comparing the value of the manual testing and the program results.

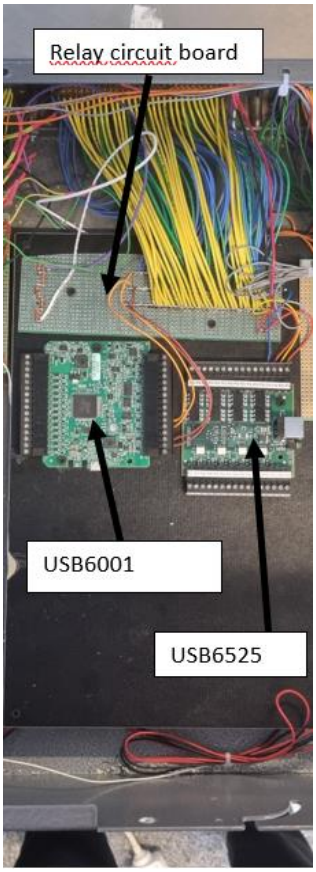

Figure 22 Hardware of the solution for the relay port.

5.3 Test Results

The tests done for each different type of channel have many different results that represent what could be faulty. The UI shows the operators the test results and explains where the fault could have occurred if there was one. Each test has multiple possible results that are shown in different ways. The program warns the operators if any results representing a faulty pin have occurred and what pin or pin pair the program was testing when the fault occurred.

The digital input/output test is the easiest to know where the error occurred because the only reason for the test to result in a fault is for one or both of the pins in the pair to be faulty or the internal operations of the platform not working. The test sends a signal from an output

into an input, creating a loop for the signal. By knowing from the test which of the pairs is faulty, the operators can manually check the pins of the pair directly. If the pins of the pair are not faulty, it only leaves the option of the platform's internal operations. This test makes it clear to the operator if the test passed, and if it did not, it makes it easy to check what the fault was. The time for the program to complete this test is swift at a maximum of 10 milliseconds for all of the DIO pins together on the DAQ port. Figure 23 shows the UI for the DIO, where a text box describes the faulty pair's location on the DAQ port.

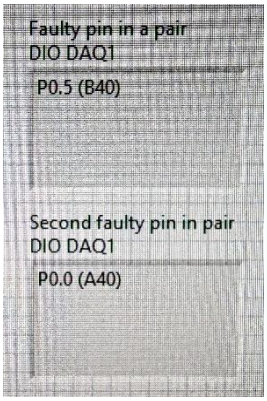

Figure 23 Text boxes on the UI that say which pins are faulty.

The digital and analog GND tests result in a digital low or high. If the test works as intended, a logical low is measured on the external device. The method segment explains how the test works. If there is a fault with the GND, the signal should be a logical high. When this happens, the signal it receives is higher than 2 V and lower than 5.8 V because the standard is TTL. The tests use an additional test to verify the outcome of the actual test. The additional test is to check if the voltage source works. If the voltage source of 5 V from the external devices used in the coupling for digital and analog GND is faulty, the results of the tests will all be logically low, and the GNDs can be interpreted as working even though some might be faulty. The test for the voltage source is just shown in the UI as a low or high LED. Figure 24 shows the analog GNDs UI, including a text box and LEDs.

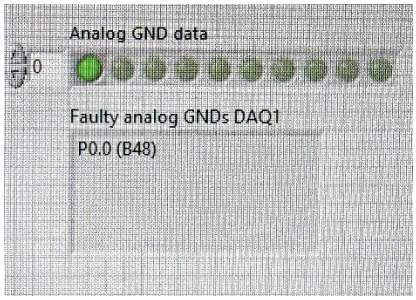

Figure 24 Text box on the UI that says which analog GND is faulty.

The analog output and analog output GND test results are visible on a graph for the operators, as well as a text explaining what the voltages of the pairs are and if a fault is present. The test is based on connecting an AO and an AO GND into a differential pair on USB 6001 to test both pins simultaneously. The pair works if the program measures a signal inside a set threshold, the threshold is set at 5.02 to 4.98 volts, and the signal should be a constant 5 V. Because there is noise from the cables and instability in the power source signal, the signal will vary by 0.4 %, and because the signal is 5 V, the thresholds are set 0.02 V over and

under 5 V. One of the results of the test is signified by the graph starting at 0 V and going up to a value under 5 V, and this means that one of the AOs is not sending 5 V or the differential input in USB 6001 is not receiving the signal and is broken. If both differential pairs are broken, the signal will start at 0 V and stay there. The difference in the results is that when one input pin on USB 6001 is broken, it is still trying to search for a signal in the air, and the closest signal is the signal from the other differential pair on USB 6001. This makes the signal with the disconnected GND get an increased voltage. When both pairs do not get any voltage, it stays at 0 V. If the AO GND connection is broken in one pair, the signal for the pair will show a floating value below the AO value, and the other pair will function normally. If both pairs do not have an AO GND connection, the value will still be below the AO but with a greater margin, as shown in Figure 25.

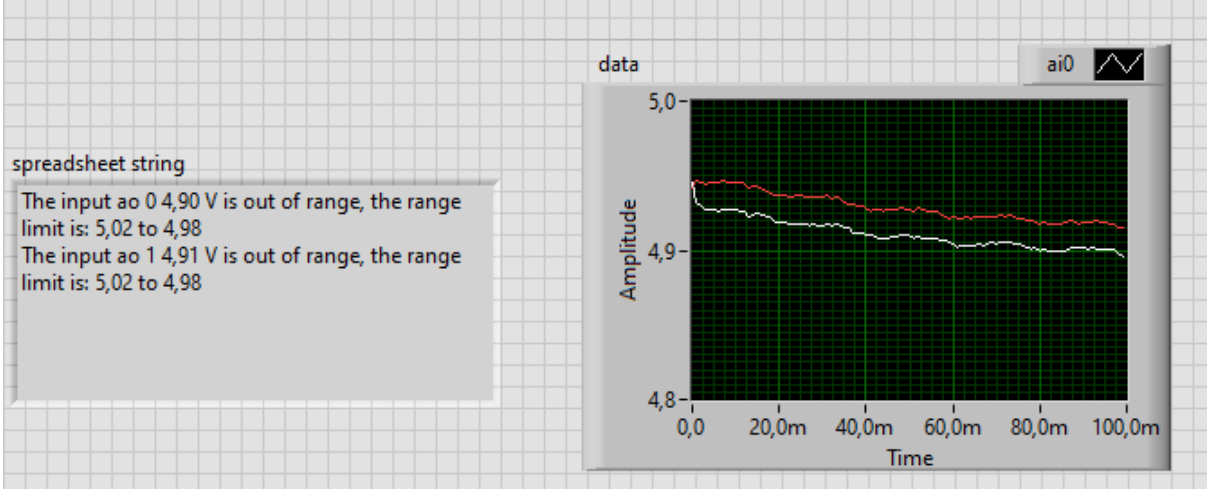

Figure 25 Text box on the UI that says if the AO and AO GND were in range or not, and a graph that shows the measured values of them.

Differential test results have three different known reasons. The first fault is that all 40 differential pairs per DAQ will show as having 1.2 volts. This is when the PSU fuse has blown and cannot deliver 5 V anymore. The PSU fuse will blow when more than 1 A flows into the platform. The test for a pair will be considered passed if the pair is measured as 5 V with a variance of ± 0.1 V. The final result is when one or both pins in a pair are broken and cannot receive a constant 5 V.
When this happens, the voltage of the test for that pair will show as a value below 4 V, depending on the inner resonance of the pair in relation to the rest of the pairs. These three known results make it clear to the operators where to check after faults. As explained in the method section, every differential pair must be tested for one second or more, and because the differential code tests 40 different pairs per DAQ port, it takes 80 seconds. Concerning the other testing programs, including the relay, the differential test takes up approximately 80 % of the total time running the test rig program. The differential test is robust because if an unexpected error occurs, the test result will almost certainly not be within the threshold and be shown as faulty. This means that a faulty coupling that delivers almost precisely 5 V is very improbable. Figure 26 shows a graph of the samples taken for the last iteration while testing the differential pairs and the text it writes when a tested pair is over or under the threshold.

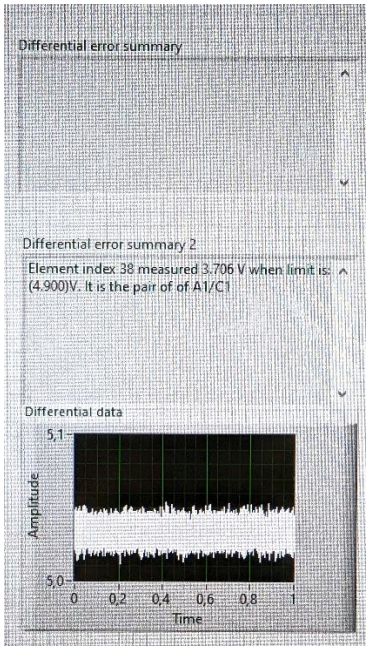

Figure 26 Text boxes on the UI that say how much and where the faulty differential pins are.

The relay port test is the same for all 32 relay channels, so only a single result must be interpreted by the operator. The result of the test will be every relay channel's contact resistance. The resistance of the channels will differ significantly, and it is the operator's decision whether the contact resistance is too much and whether it should be fixed. The higher the contact resistance, the greater the risk that the switch in the relays will break or that the current flowing through the relays will be too small for when the relays are used for PCB testing. The relay's contact resistance is 40 to 50 $m\Omega$ when it is new, but as seen in Figure 26, which shows some of the channels' contact resistance, some relays have resistances as high as 250 $m\Omega$. The operators must decide when the contact resistance is too high and when it must be fixed.

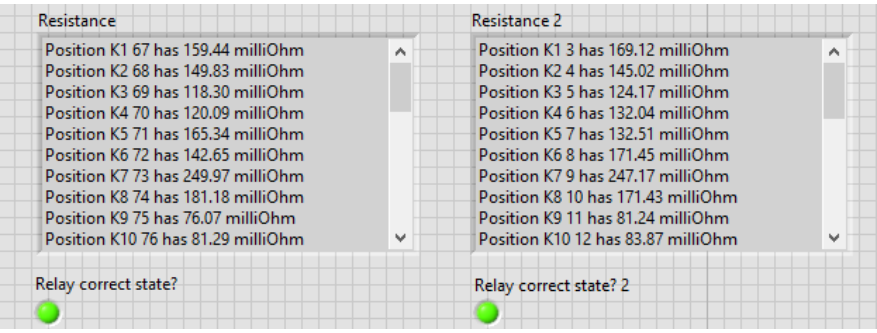

Figure 27 Text boxes on the UI that say how much contact resistance there is between the input and the outputs in the relays. There is also the error in, and error out that will write out the unexpected errors of the program if such occurs.

5.4 Analysis of Results in Context of Goals

The results of the tests in relation to some of the project goals are significant because of how the results conform to and impact the goals and requirements of this project. A goal of the project was for the results to be easily interpreted by an engineer. The UI is made so that the operators can read the text boxes of the tests and go and get an HMS engineer who will check

what specific fault it is depending on the results. The UI lessens the need for knowledge concerning the tests performed while still having enough information for a person with expertise to analyze.

As mentioned and described earlier, the test results must have a way to determine if the input or output being tested passes or fails. Each test has a preset value or state representing that the test passed. The preset values were chosen because they are the expectation of the coupling output when a specific input is used. The program for each test compares the measured values to the preset values, which is the result. Quantitatively, the results indicate whether the test has passed. If it has not, the results also provide insights into why it did not pass.

The known results explain how to interpret them and why they occurred, but there could be and probably will be faults that can occur that are currently unknown. The unknown faults are not included in this thesis project and will not be accounted for. The way the program handles unknown faults is to signal them as faults if they can detect them but with no way to interpret the result. If this occurs and an engineer tries to fix the platform's perceived fault, it will not fix anything. The unknown fault could also pass the test but actually be faulty and not detected by the tests. An example of this could be an input channel that can measure voltage correctly but not current.

5.5 Project Results

The finished product is a test rig that tests the DAQ and relay ports. The port couplings are integrated into a single test rig, and the designed code runs seamlessly between the tested ports and outputs an easily read report of the status of every pin. The test rig is lightweight and robust enough for excessive use. The PCBs and external devices being screwed onto the carbon fiber plate make the test rig very physically robust even after excessive use and external forces, which was one of the goals. In addition, the pins on the PCBs and the external devices have been appropriately soldered to reduce the risk of losing connection or detaching from the board. The test rig has space left for more ports to test. Figure 28 shows the finished test rig with all circuit boards and devices mounted onto the test rig.

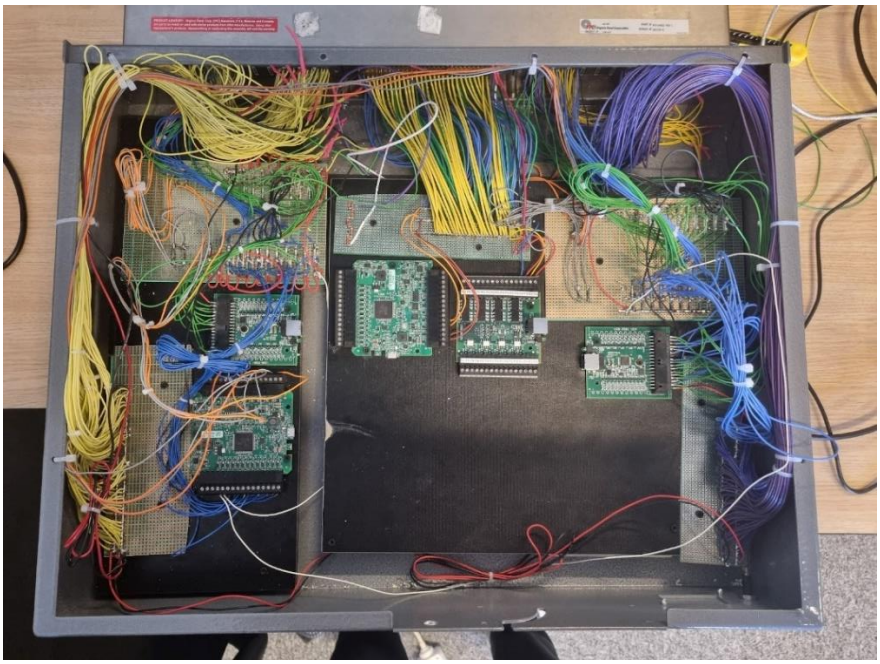

Figure 28 Completed hardware coupling of the entire test rig.

5.6 Noise calculations

The thermal noise in the cables disturbs the signals in this project and, therefore, can change the actual values of the channels. However, since the thermal noise is relatively small, it primarily affects the analog signals.

The thermal noise is calculated using Equations 3 and 4. The temperature is approximately 20°C, and the bandwidth of all platforms is 1.7 MHz.
To calculate the resistance in the cables Equation 1 is also needed. The cables used for DIO, GND, AO, and AO GND and differential is an Alpha wire ecowire TM 22 AWG 600V, which has a resistance of $16.2\Omega/1000ft \approx 53.15 * 10^{-3}\Omega/m$ @ 20°C. The cables used for the relay and from the PSU are Alpha wire ecowire TM 20 AWG 600V, which has a resistance of $10.6\Omega/1000ft \approx 34.78 * 10^{-3}\Omega/m$ @ 20°C [28], [29].

Table 2 Thermal noise calculations in the different cables as well as the thermal noise in the resistors.

Type	Resistance (mΩ/m)	Length approx (m)	Resistance (mΩ)	Noise [nV]
DIO cable	53.15	0.22	11.69	17.93
GND cable	53.15	0.85	45.18	35.24
AO and AO GND cable	53.15	0.75	39.86	33.11
Differential cable	53.15	0.90	47.84	36.27
Relay cable	34.78	0.20	6.96	13.83
PSU cable	34.78	0.95	33.04	30.14
Resistors	-	-	$1500*10^3$	6422

The reasons for the different resistances are partly due to the two types of cables in this project. The cables connected to the Relay and PSU port use American wire gage (AWG) 20, while cables connected to The DAQ port use AWG 22. AWG 20 cables have a cross-sectional area of 0.519 mm^2, while AWG 22 cables have a cross-sectional area of 0.324 mm^2 [30]. According to Equation 4, the larger the cross-sectional area, the smaller the resistance. In addition, some cables in the test rig are much longer due to placement in the test rig than others, which also increases the resistance and, therefore, the thermal noise.

Even though some thermal noise in the cables affects the components, they are not large enough to make a significant difference in the analog signals. When GNDs are being tested, they use a 5 V power source, and the noise is 35.24 nV, which is $1.762*10^{-7}$ % of the power source's signal or 163dB below the measured signal, according to Equation 10.

Equation 10 Formula to convert a ratio between signals into db. V_1 is the signal of 5 V and V_2 is the noise of 35.24 nV.

$$20 \log \frac{V_1}{V_2} \tag{10}$$

The thermal noise in the resistors is approximately 200 times more prominent than the cables, but their noise, like the cables', is still insignificant in the measurements in the test rig. It is also worth noticing that the thermal noise for the relay cable is between one-half and one-third of the size of the other thermal noises, which is essential since one of the goals was to have as little disturbance as possible when the relays were being measured. Because of this, the deviations in the signals on the test rig must also come from the thermal noise within the components, ripple noise from the platform, and the unsteady signal from the power sources.

The resistances of the cables could have been measured if more precise multimeters existed at HMS. When measurements were made, the multimeter showed 0.2 Ω for the cables, which is highly unlikely. It was noticed that the 0.2 Ω was the multimeter's internal resistance, as shown in Figure 29. Because of this, the different cable resistances could not be measured using a multimeter.

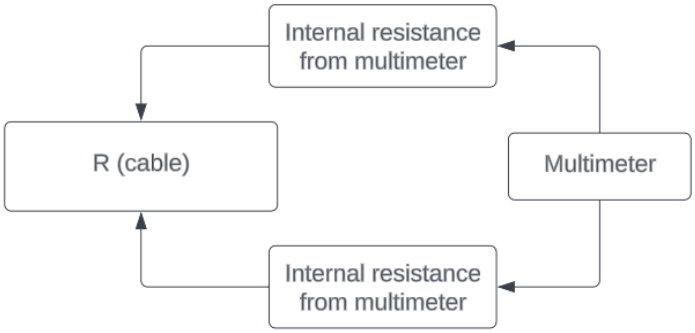

Figure 29 How the cables' resistance was being measured.

If more time existed, this could have been solved by sending a known current through the different cables and measuring the voltage drop over it using a voltmeter to get a more accurate result, as shown in Figure 30.

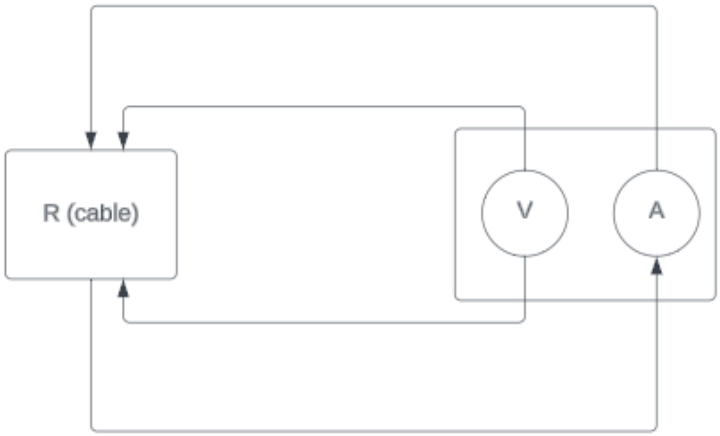

Figure 30 An idea to measure the cables' resistances by sending a known current and measuring the voltage drop over the cables.

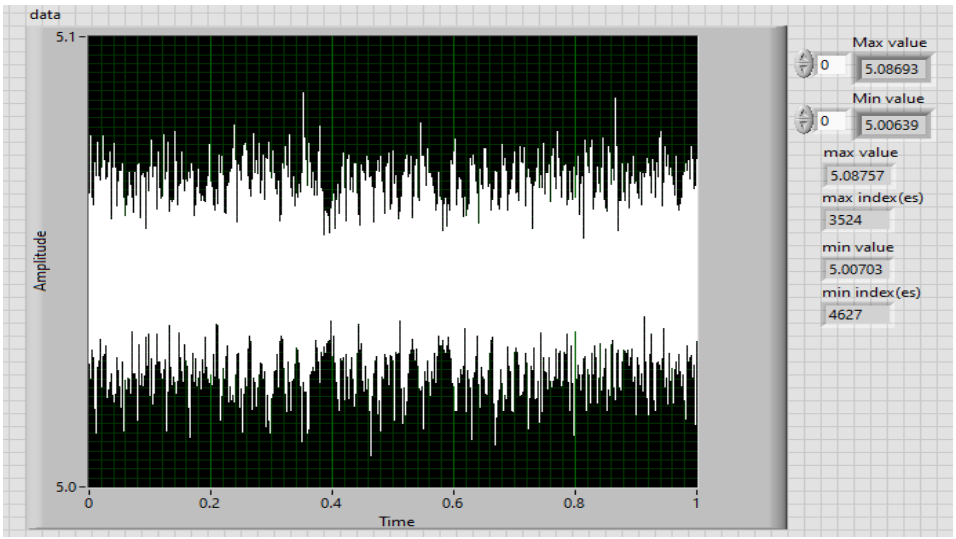

Figure 31 The deviations in an analog signal that receives 5 V from the power supply.

As shown in Figure 31, the analog differential signal deviates between 5.00639 V and 5.08693 due to the thermal noise within the cables and the soldering on the circuit board. The deviations can also come from the instability of the PSU, where a ripple noise of around 1.5 mV can occur. In addition, the DAQ port's analog input has a 157 µV random noise at a 5 V input. Some noise may also arise where the signal is connected between the test rig and the platform, which is the physical pin. Moreover, the PSU should also be calibrated once every year for more precise signals. However, this has not been followed at HMS because precise signals are not the most interesting from the PSU, according to HMS's engineers. Due to this, the majority of the noise is from the lack of calibration [31], [1].

6 Discussion

6.1 Result Comparison

The built test rig and the program in LabVIEW test all pins on the DAQ and relay port and compare them to set values if they pass or not, as well as calculate all the resistances in the relay port, which is in line with the set goals of the project.

The result of the resistance calculations of the relays was a success. However, the project's resistances are only calculated by switching a relay once and calculating its resistance. In the study “A Universal Life-Test System for Electromechanical Relays” [9], they calculate the resistance for a relay for multiple switching frequencies to examine if the resistance changes. The contact resistance may change with different frequencies as the switching may affect the relay with light arcs during intense switching. To calculate the resistance of the relay in their study, they used Ohm’s law, just like in this test rig project. The problem is that they approximate the current when the calculations are done according to their software code instead of using the exact measured value. Therefore, the test rig project will give a more accurate resistance calculation than the study does as it divides the voltage drop by the exact measured current through the relay, not an approximation as they do.

To test if the pins on the DAQ ports are faulty, signals sent to or from the DAQ port are measured and compared to set thresholds in the software. The signals used to test the DAQ port are commonly used in a platform’s typical operating environment. This way of concluding whether a pin passes is the same way the manufacturing companies VSE and PCBgogo test their PCBs before selling them to their clients. They perform a PCB functional test, which includes sending signals to the PCB that are expected to come during the PCB's operating environment.

A stress test could be performed to further test the quality of the pins in the test rig project. The measurement and instrument company Kiethley Instruments conducts continuity tests on the pins of their PCBs to stress the pins by sending a current well over its rated current, which will verify the pin’s performance margin. The test rig does not conduct a stress test on the pins, so it does not check what would happen if a signal outside of its operating environment occurs. However, if a signal well outside the typical operating environment appears, the test rig would still notice it from the programmed code, write out which pin the signal came to or from, and write that the pin is faulty. The other way would be for the error handler to notice. For example, the AO pins have an output current drive of ±5 mA and an overdrive current of ±26 mA. A stress test on the AO pins could verify if it can still reach +-26 mA if the overdrive current is needed [23], [24], [22], [1].

In the study “Complete, Contactless I/O Testing - Reaching the Boundary in Minimizing Digital IC Testing Cost” a test was conducted on I/O pins to calculate their leakage current.

This test started with connecting bi-directional pins and set one as input and the other as output. The output would then send a signal, and the input would receive the output value. This part of their test is very similar to the test rig's test on the DIO pins as they are also bi-directional, and the output sends a value to the input. The difference is that the study takes their test further by being able to test the pins in parallel, which is more effective, as well as calculating the leakage current of the pins. Calculating the leakage current of the pins on a platform in the test rig project could have been a good improvement to the project. Calculating the leakage current on a platform would have shown the operators if any pins do not have sufficient insulation. Insufficient insulation or a leakage current that is too high can result in the PCBs typically tested by HMS not getting the right signals from the platforms.

6.2 Strong and Weak Points with the Implementation

The test results implemented to test a platform's ports have some disadvantages. The results of the tests all have some minor problems that fixing would make it easier for the operators to interpret the results and speed up the testing. The biggest problem with how the results are shown to the operators is that the operators have to be able to interpret the results and have basic knowledge of the tests to understand the results. Also, the digital measurements of the tests create a problem where only two possible outcomes are low or high. The problem is that it is still high when the digital input measures an input that is 4 V when it should be 5 V. This makes it possible for the signal to be wrong but still result in the correct logical state.

The DIO and the differential tests have a problem where if one channel in the pair being tested shows as a pair, it is impossible to know which pin in the pair is broken, so the operator must manually check both pins in the pair. The GNDs have a problem where the input signal could be faulty instead of the GND, which will show the result as the test has passed. If the operators do not find any error with the program-flagged pins, the error may be caused by the platform's internal operations. If the problem is the internal operations of the platform, it could be affecting other tests. If it is an internal problem, it could be picked up by the error handler, and as mentioned in the Negative Testing section, the error handler will write out what and where the problem is so the operators can fix it.

The differential test is clear to the operators, as explained in the Test Results segment, but the time required for the test to be done is very long compared to the other tests. The project aims to have the test take as little time as possible, but no explicit time limit is set as to what time is the maximum. The project is meant to alleviate time spent manually looking at pins on the platform. The difference between the project's solution and the checking of pins manually is that the test can run automatically and only has to be started to run on its own. The other test rigs that test PCBs can run their whole program for up to 30 minutes before completion. Because the test rig runs automatically and it is easy to start the test program, an operator can do the test instead of an engineer. In addition, the operator connecting the test rig with the platform does not need to monitor it and can do something else while the test rig runs the

code. The current runtime for the whole program containing all tests takes approximately 100 seconds. Therefore, the little time it takes to run the entire test rig program is not a problem.

The reference GNDs are connected to the external devices in the couplings and are used to create a common ground plane that the digital inputs and voltage sources use as a reference for the signals they measure. The reference GNDs are not tested, and when they are faulty, the signals measured as GNDs are instead a floating value measured from the air. This makes the other tests, such as AO and AO GND, a floating value that is not precise.

A strong point with the implementation is that the test rig also checks the power sources from the external devices to conclude that there are no errors with them. If this is not checked, the test rig could write out faulty messages, such as all GNDs being low even though one might be faulty and should, therefore, be high on the test rig's UI. Furthermore, the noise and resistance in the cables have been held to a minimum to affect the measurements as little as possible, which is in line with the goal set at the start of the project.

The robustness of the designed tests is excellent. The robustness has been tested by running the program more than 100 times with or without simulated faults, and the program has been right on every single iteration of the runs. This accuracy in determining results lets operators at HMS trust the test results and have confidence in calling in an engineer when the program detects a fault.

Lastly, the code in LabVIEW and the physical coupling are relatively easy to understand and, therefore, easy to change if necessary, as might be the case in the future at HMS. The code has clear names for the different VIs, controls, and indicators that say what they belong to and what they do within the code. The code also consists of multiple subVIs for the different tasks of the project. Thanks to the subVIs, debugging and making changes if necessary, is more straightforward than having a giant code that does everything, which can be messy and complicated to interpret. As mentioned, the physical coupling is color-coded, making it easy to see what every cable is connected to within the test rig.

6.3 Improvements

The project results meet the set goals, but there is room for improvement in the methods used to achieve these goals. The most significant improvement that could be made to the project is to create PCBs instead of soldered circuit boards when the couplings have been confirmed to work. This would reduce the amount of cables needed and would require less space. If the circuit boards were PCBs, cables would only need to be connected to the platform and the external devices. This would lower the space required by the couplings because PCB wiring and component design are much more effective. The cables could also be shorter and more efficient because the PCBs and external devices could be placed closer to each other. This would lead to a simpler-looking test rig and contribute to an easier understanding of the couplings.

The circuit board couplings were not made into PCBs because designing PCBs takes time, in addition to the need to be able to print them. When talking to HMS engineers about designing PCBs instead of, or after verifying the coupling works, it was decided that this was not a priority. To design a PCB, it is necessary to learn the program and the standard used by either HMS or another company that prints PCBs. If a PCB stops working, the only time-efficient thing to do is print a new one. Soldered circuit boards are the opposite. It takes longer to make each board, but if something breaks, it is easier to replace it.

Moreover, the resistance of the relays can get a more accurate value if the cables to the relay were shorter, had less resistivity, and had a larger cross-section area. Every cable takes up some voltage and current, but that is not included in the calculation for the resistances, which gives some excessive resistance. The cables should be shorter to achieve a more accurate value, and their resistance should be included in the calculation.

Another improvement that could be made for the project is to increase the efficiency of the code. Instead of running the code in series, first DAQ 1, then DAQ 2, and lastly the relay port, the three parts could be run in parallel to decrease the amount of running time. This has not been done in the project due to the time needed. The different task VIs named DAQ.mx that existed in LabVIEW before the project cannot be run in parallel. However, it is possible to build new task VIs that could run in parallel, but there was not enough time to learn and execute this. Furthermore, if such VIs were to be made, they could come with problems such as encountered on the differential where rapid testing increased the voltage of a pin on those faulty due to resonance within the platform itself and could, therefore, be interpreted as not faulty.

In addition, more efficient or external devices with different input/output pins could be used. However, HMS wanted the external devices they already had in storage to be used and pointed out that external devices are costly for the company. If prices were not a problem, an external device called USB 6218 [32] from National Instruments, which costs approximately 26 000 SEK, could replace the two currently used USB 6001 in the test rig, which costs approximately 3400 SEK each. This would decrease the number of devices and space used in the test rig. Furthermore, USB 6255 [33] from National Instruments, which costs approximately 57,000 SEK, has 80 analog inputs and could replace many external devices in the test rig. If USB 6255 were to be used, every pin would be measured with analog instead of digital signals. This would give a more accurate result for the pins on the platform. When measuring digital signals, all voltages under 0.8 V are a logic low in USB 6501. This would mean that a GND could be 0.7 V instead of 0 V, but it would still show low on the interface using digital measurements. If analog measurements were made, this increasing voltage and deviation could be monitored if other external devices were to be used.

Lastly, the color coding for all the cables could be improved. The colors for the cables on DAQ1 and DAQ2 should be the same, but there were not enough cables in unique colors at HMS to make this possible. Therefore, some cables look different even though they send or receive the same signals in DAQ1 and DAQ2. Because of this, troubleshooting of the cables will be more difficult. The color coding for the relay encounters the same problem. There are different types of cables and physical pins that go into the DAQ ports and the relay port, and because of this, the cable colors were not enough, and some colors already used for the DAQ ports had to be used again for the relay port. Every type of signal should have its specific color to represent it, which will ease troubleshooting and be more consistent.

6.4 Societal Requirements

The project aims to save time for engineers at HMS by freeing the time spent checking after problems on a platform and making this more efficient. Checking if a platform is broken takes varying amounts of time, but every check takes at least 30 minutes.
The platforms are a universal HMS Networks testing tool, and there are many platforms globally. All these platforms are regularly checked, which takes up a lot of time. If this time could be removed or drastically shortened, it would allow HMS engineers to dedicate more time to creating or updating other testing equipment to make it easier for the operators using the platforms to do their jobs.

This time reduction would enable HMS to save money and make them more profitable. Making HMS a more profitable company helps the environment because HMS has a gold rating by ECOVadis and is a signatory to the UN Global Compact. Additionally, HMS's core aspects are that it is a company that focuses on energy efficiency, human rights, and keeping customer data protected, to name a few. This means that HMS is a sustainable and responsible business that helps society move forward in the right direction [34].

6.5 Future Work

If this project had continued, the major future work would have been the addition of more ports. This project limited itself to two of five different ports. The remaining ports could be designed and developed similarly to this project. Besides working on more ports, improving the existing ports mentioned in this report is also possible. Additionally, the set testing values could be changed from a constant value to a control value to make it easier for the operator to change the values in the interface if HMS wants the operators to be able to change them for different tests.

6.6 Conclusion

The project group built and programmed a test rig for HMS to test the pins and relays of the DAQ and relay port on their testing platform. With the help of a programmed interface, the platform operator at HMS can easily see where and what the problem is if one should occur. Thanks to its color-coding and well-structured programming, the engineers can easily change the test rig's hardware and software if needed.

Overall, the project results were a success. It is possible to determine if any pins are faulty and help the operators and engineers save time. The results also matched the project goals set during the halftime seminar. The project goal of not taking too much time to run the tests has been met, as discussed in the Test Results section of the Implementation segment. The goal of having as little noise disturbance as possible for more accurate measurements has also been met, as mentioned in the Noise Calculation section of the Implementation segment. The goal of quantifying the results has been fulfilled, and explaining how the goal has been

completed is in the Method segment. The quantification of the methods used and how to interpret the results are described in the Implementation segment.

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8 Appendix

Table 3 Electrical characteristics for AO-channels on DAQ

Number of channels	2
DAC resolution	16 bits
Timing accuracy	50 ppm of sample rate
Timing resolution	10 ns
Output range	± 10 V, ± 5 V
Output coupling	DC
Output impedance	0.2 Ω
Output current drive	± 5 mA

Table 4 Electrical characteristics for AI-channels on DAQ

ADC resolution	16 bits
Maximum sample rate	500 KS/s
Timing resolution	10 ns
Timing accuracy	50 ppm of sample rate
Input coupling DC	Input range: ±0.1 V, ±0.2 V, ±0.5V, ±1V, ±2V, ±5V, ±10V
Maximum working voltage (signal + common mode)	±11 V of AI GND
CMRR (DC to 60 Hz)	100 dB
Input bias current	±100 pA
Crosstalk (at 100 kHz):	
Adjacent channels	-75 dB
Non-adjacent channels	-88 dB
Small signal bandwidth (-3 dB)	1.7 MHz

Table 4 Electrical characteristics for AI-channels on DAQ

Input FIFO size	4,095 samples

Table 5 Electrical characteristics for AI-channels on DAQ

Scan list memory	4,095 entries
Overvoltage protection for all analog input and sense channels	
Device on	±25 V for up to two AI pins
Device off	±15 V for up to two AI pins
Input current during overvoltage condition	±20mA max/AI pin

Table 6 Electrical characteristics for the relay port

Minimum operating voltage	18 V
Typical operating voltage	24 V
Maximum operating voltage	30 V
Operating current at 24V DC	390 mA
Power dissipation at 25°C	3 W
Rated current	2 A
Maximum switching voltage AC	400 V
Maximum electrical operation frequency	1800 cycles/h
Contact resistance	<50 mΩ
Operate time	5 ms
Release time	2 ms
Bounce time	1 ms

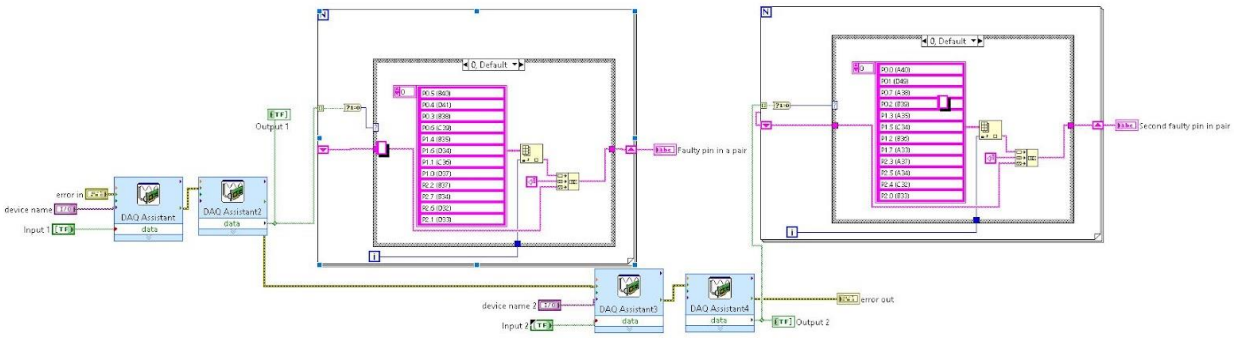

Figure 32 Digital Input/Output block code schematic.

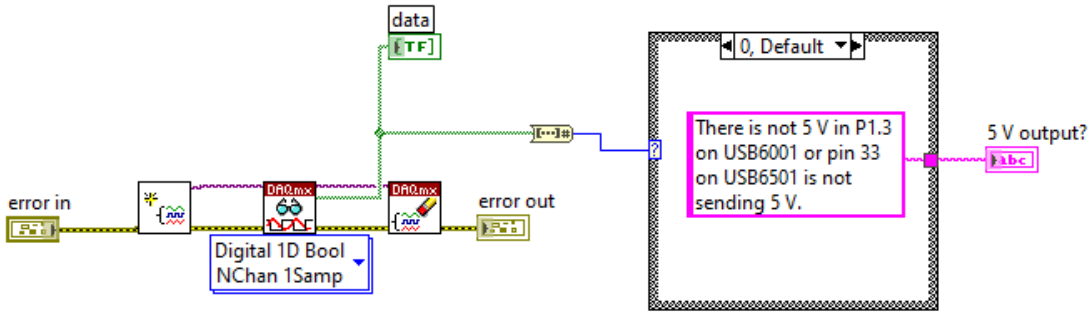

Figure 33 V tester block code schematic.

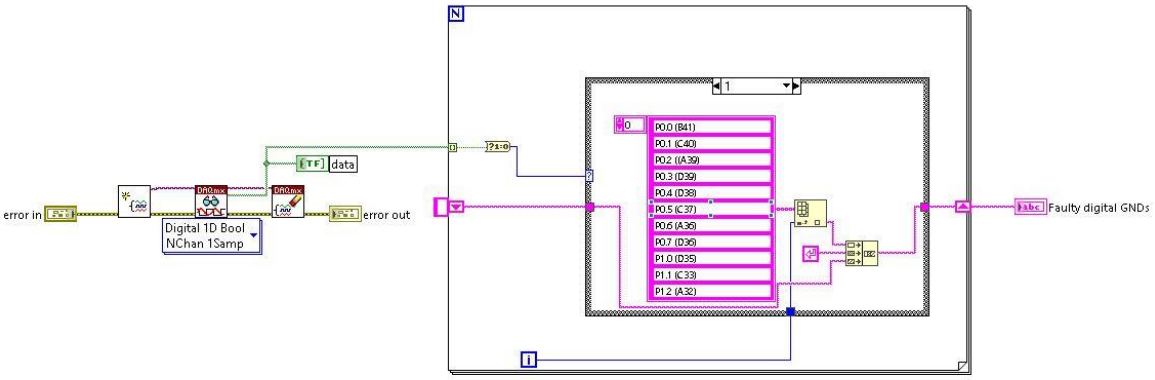

Figure 34 GND block code schematic.

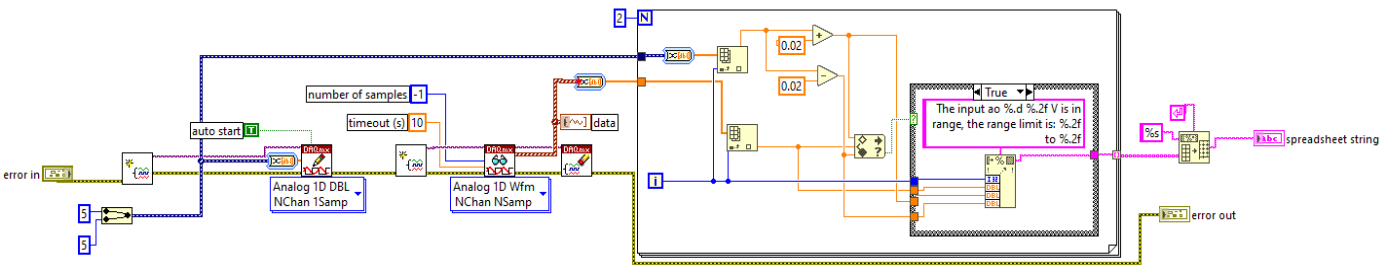

Figure 35 AO and AO GND block code schematic.

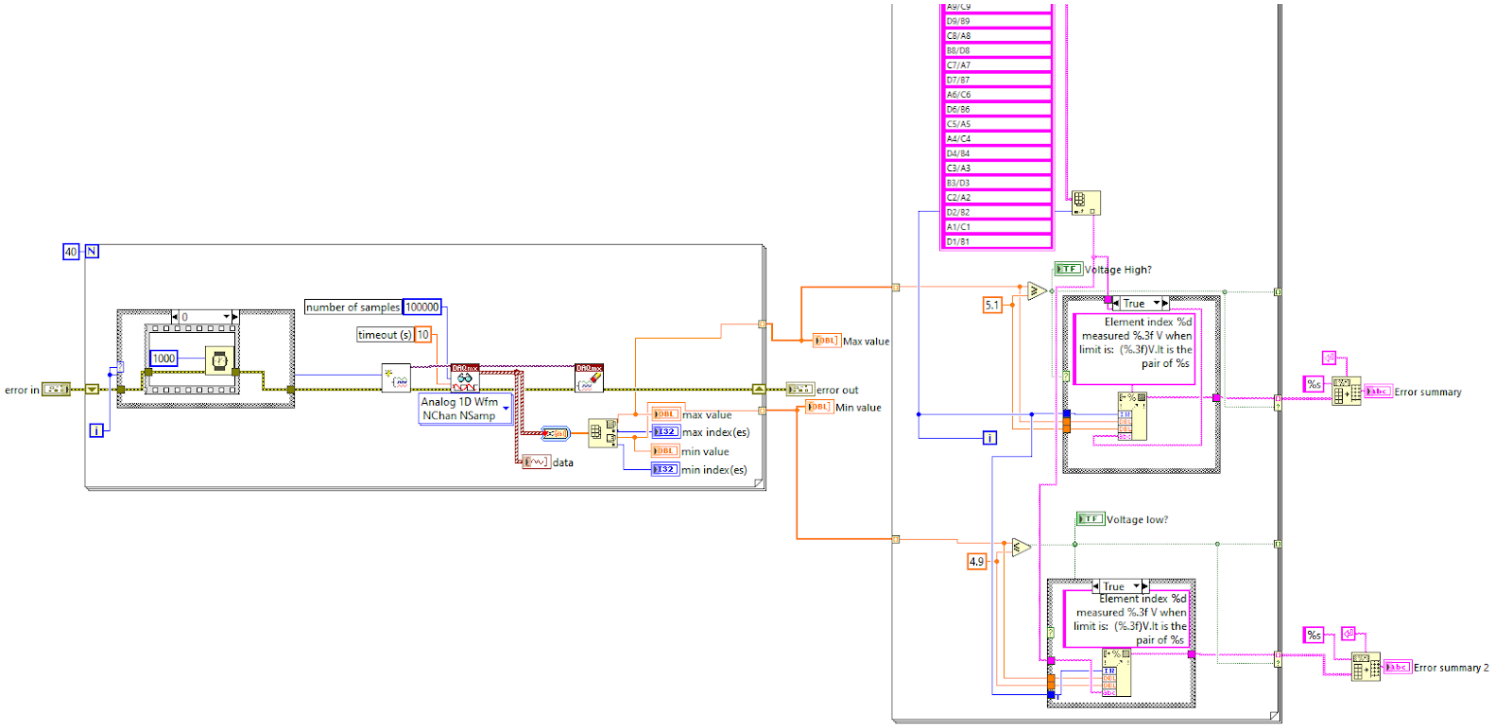

Figure 36 Differential analog input block code schematic.

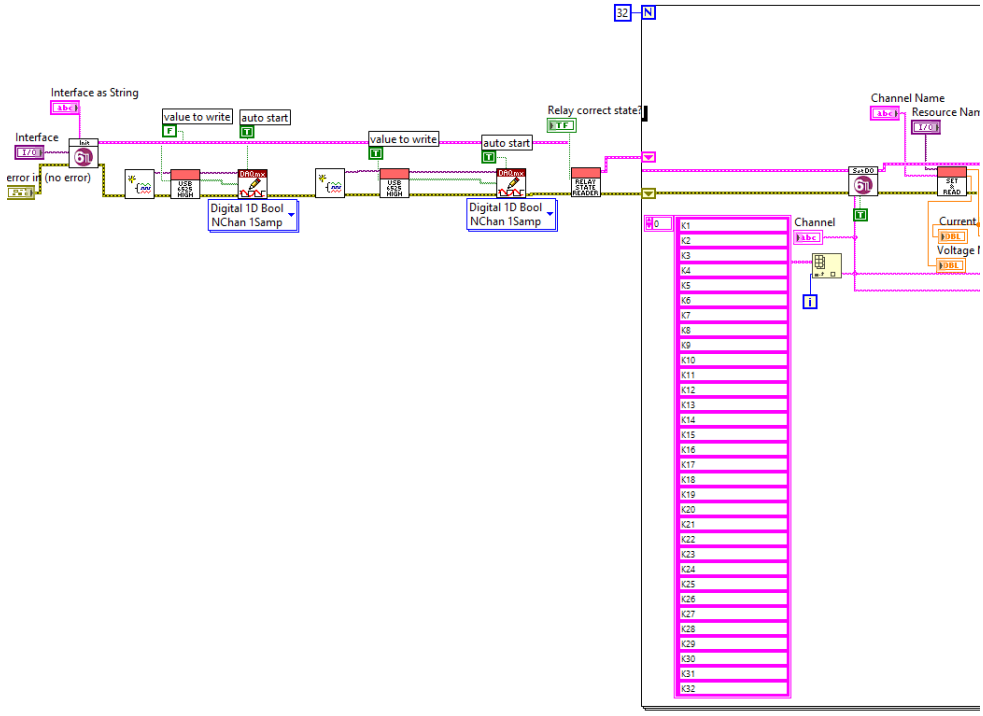

Figure 37 Block code schematic over the relay. Note: Figure 37 is the second part of the entire program.

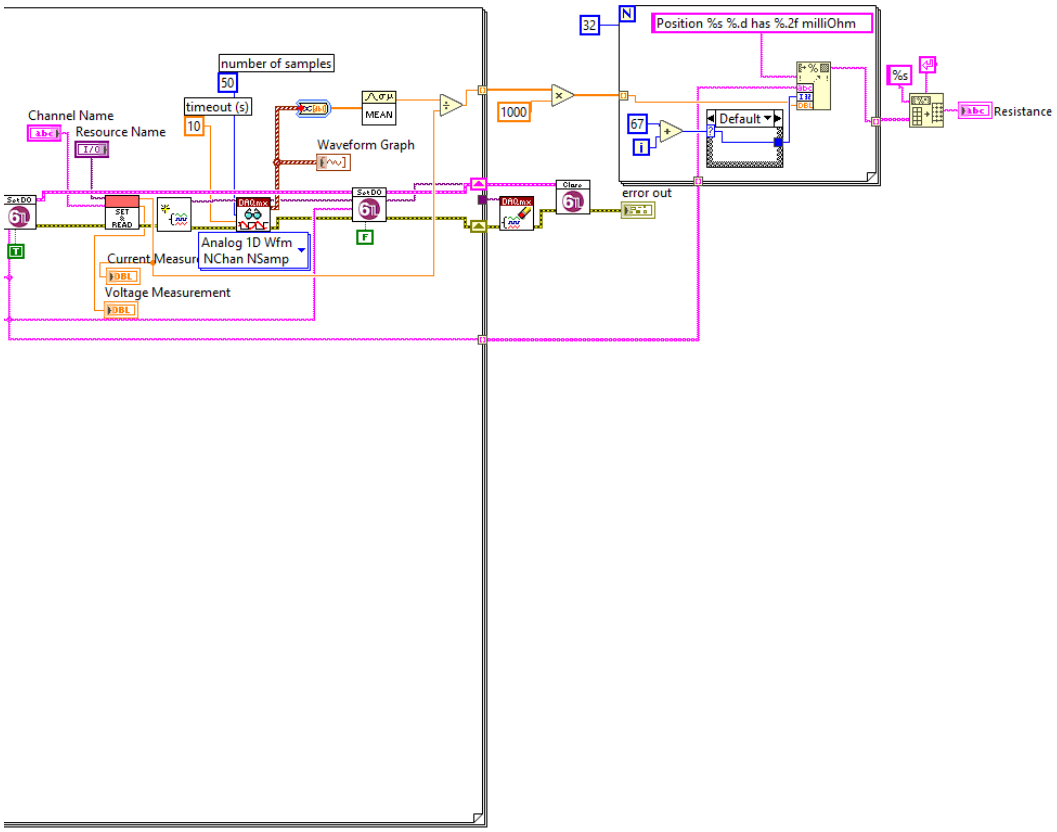

Figure 38 Block schematic over the relay. Note: Figure 36 is the first part of the entire program.