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A New CMOS Radio for Low Power RFID Applications

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***Abstract*—A novel radio receiver circuit, functioning as a tuned active, detecting antenna, is described. The receiver is suggested to be part of a new radio system with the potential of competing with the range capability of active RFID-tags and, through its low power and long lifetime, with passive RFID-tags. The circuit is outlined and the functionality is verified by simulations and measurements.**

A 24 MHz discrete prototype showed better than -70 dBm sensitivity and 5 kHz bandwidth, with a power consumption of 102 µW. Simulations of a monolithic implementation were performed at 2.5 GHz. The detector is modeled by using 180 nm CMOS transistors. In simulations the power consumption for the detector is below 125 µW at a sensitivity of -83 dBm and a bandwidth of 9 MHz.

Our conclusion is that this novel simple circuit architecture is well suited for monolithic implementation of a low power transceiver.

I. Introduction

In the context of power consumption of radio electronics, it is interesting to notice that almost all transceivers available today are based on the superheterodyne architecture [1]. The superheterodyne has superior performance when it comes to sensitivity, but as monolithic integration and power consumption has come into play, the direct conversion receiver has become increasingly popular. The super-regenerative receiver is another alternative suggested for cheap, low data rate, communication [2].

We propose a new radio technology, a system based on a receiver constantly in operation in low power mode. The basic idea of the technology is a resonant circuit changing from a low power, stable non-oscillating state to a second state of self-oscillation by excitation from an aerial radio pulse. This system has no need for a complex communication protocol with synchronization.

An example of a class of applications where this is particularly important is active RFID. In many cases we require very rare access to the tag, but when this happens the access time must be kept to a minimum. The fact that the tag detects change of energy level instead of phase of a modulated signal leads to a very simple design with no other silicon components beside the radio chip itself. RFID applications have an asymmetric requirement on power consumption regarding the central reader and the distributed transceivers, which can be used to minimize complexity in transceivers by placing excessive power consuming functionality in the reader.

Long-time operation of short range radio systems using limited energy sources requires low duty cycle operation, meaning a long sleep mode time period. However, the response time of the system increases with the length of the sleep mode time period, which excludes radio applications involving real-time coordination and control. Furthermore, low duty cycle introduces a large clock drift. As a result, more guard space is needed in order for the clock drifting stations to be able to rendezvous in time. A related problem to clock drift is that the start-up time of a transceiver is of the order of 100 µs [3] (going from sleep mode to active mode). The actual transmission burst in this kind of applications often takes less than 100 µs, this indicates a lot of overhead of power consumption for each initiated transmission.

Performing rendezvous in time, means scheduling the time of activity. This implies the necessity of accurate time synchronization in-between all stations, to perform synchronized wake up. Synchronization is especially difficult in low power consuming embedded systems, since the clock drift in such devices often is substantial, especially when they are put in some form of low power sleep mode. High clock drift can either be compensated with a high frequency of synchronization message exchange or with large guard space in the time domain for the rendezvous. The transceiver which is in receiving mode is the one which has to add a guard space; otherwise it may miss parts or the entire transmission from the transmitting station. A typical drift value for a good clock is ±50 ppm [4], but for a low power integrated RC oscillator used in sleep mode it can be in the range of ±1000 ppm [5].

To be able to be in listening mode all the time receivers used in wireless networks should have a power consumption in the order of 100 µW [6]. Recent work show just below 1 mW of power consumption each for LNA's and mixers made with CMOS technology at 5 GHz [7]. At 2.4 GHz the figures are 500 µW and 400 µW for LNA and mixer respectively [8][9]. Oscillators in CMOS have been demonstrated running at 100 µW to 300 µW at 1.9 GHz [6][10]. Recently published papers demonstrate the use of simple envelop detectors for low power wake-up radios with external networks for improved selectivity [11]. The drive to minimize cost by reducing the number of components in the transceivers excludes the use of low loss, high Q-value off-chip components such as crystals. For small chips the silicon area saved by using external components is actually significantly reduced by the extra pads needed [12].

Our proposed low power detector is listening without a

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running local oscillator (LO). It is in constant operation without duty cycling, thus enabling a short response time. To make full use of the functionality of this new detector, a new protocol for communication has been developed. The protocol is of the binary tree type, meaning that the ID is extracted bit by bit when traversing a binary tree detecting whether the tag's next ID-bit is a '0' or a '1'. To extract bits in the tag ID, the protocol uses frequency signalling. The tags in the vicinity of the reader are first awakened by a beacon signal. The awakened tag's IDs are extracted by using four different frequencies, where every frequency corresponds to a two-bit combination in the ID. A detailed description is found in [13].

This paper is organized as follows; II) Description of the receiver design. III) Model of the receiver. IV) Simulations and measurements. V) Conclusion. VII) Future work.

II. DESCRIPTION OF A NOVEL LOW POWER RECEIVER DESIGN

A. Actual operation

The receiver circuit in Fig. 1b is coupled to an external source, Z0 and iin. When the receiver is listening there are no oscillating currents or voltages within the circuit. The external source excites the receiver with an energy pulse at radio frequency, the source being an antenna or a low noise amplifier (LNA). Matching is performed with an impedance transformer T1, with losses included as resistors R1 and R2. The excitation pulse brings the receiver into oscillation, and the oscillations are sustained by the transistor pair M1 and M2. Energy oscillates between the inductance formed by T1 and the capacitance formed by transistor parasitics and tuning capacitance C1. The oscillation, and thereby the radio pulse, is detected as an increase in current drawn from the supply. By varying capacitor C1 the receiver can bee tuned to a specific frequency.

B. Principle of operation

The new receiver is based on an oscillator with nonlinear response to external signals. The oscillator is biased close to its periodic steady state of oscillation [14]. The design has close similarities to the regenerative or super-regenerative receivers [15]. A basic model of an oscillator is seen in Fig. 1a and is described in more detail in Section III.

There are two intended states of operation for the receiver, an idle state, where the receiver is armed and waiting for an input signal, called state A, and an active state, in which it has received an input signal and therefore is oscillating called state B. Fig. 2 shows a response from a nonlinear device with the resulting gain at two different biases, conceptually corresponding to the two different states. State A corresponds to a bias point with lower gain, gm,A=ΔiA/ΔuA. State B corresponds to a bias point with higher gain gm,B=ΔiB/ΔuB. The nonlinear response is essential for the ability to achieve stability in each of the described states.

The nonlinearity is used for keeping the receiver at a stable equilibrium point when the input signal contains too little energy in the relevant frequency band. Out of band signals are discriminated by the tank circuit. When an input signal is applied, the average current of the oscillator is increased, following the path of the nonlinearity, marked by an arrow in Fig. 2.

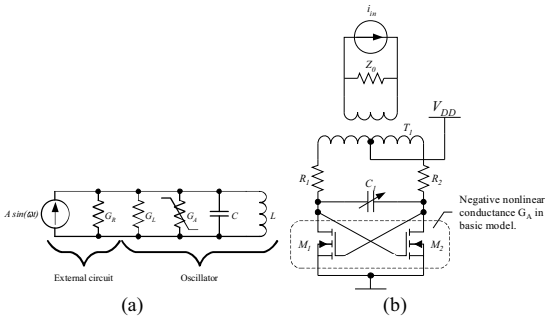

Fig. 1. Basic model of oscillator (a), and receiver circuit model (b), both with an external current source and an external load. Details about the models are found in Section III.

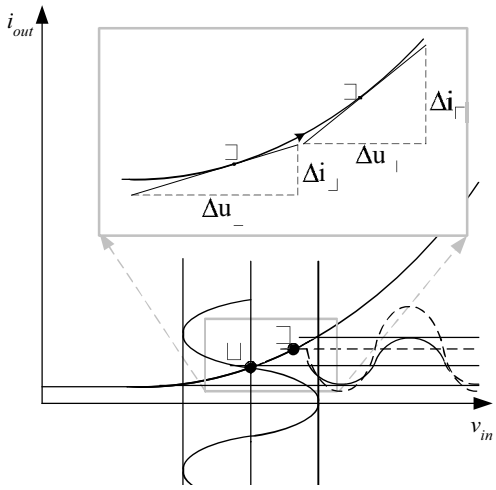

Fig. 2. Nonlinear response from an active device and the small signal gain at different bias points. The gain $g_m=\Delta i/\Delta u$ changes as the point of operation is shifting.

The gain will be too small to build up and sustain an oscillation from noise at state A. However, when the incoming pulse contains sufficient energy, the effective bias is gradually pushed toward state B, where an oscillation is created which sustains even when the exciting pulse vanishes. The necessary energy in the incoming pulse that may change state of the receiver depends on the nonlinear function of the active device, as well as on the Q-value of the tank circuit.

III. MODEL OF THE RECEIVER

A. Basic model

An oscillator model, coupled to an external source, and its parameters are depicted in Fig. 1a. The natural frequency of oscillation is determined by the tank circuit consisting of the inductor L and the capacitor C. Losses are bundled into a conductance GL, radiation conductance is represented by GR. The active device necessary to overcome losses in GL and GR is modeled by the conductance GA, characterized by a negative conductivity. In reality GA must be a nonlinear element, limiting the oscillating peak amplitude. A stronger external coupling gives an increased signal level, but also higher losses due to the external loading and thereby a need for higher negative conductance GA. The incoming aerial radio pulse is modeled by the current source.

The differential equation for the voltage u across the circuit is [15]

$$C\frac{du}{dt}+Gu+\frac{1}{L}\int udt = A\sin(\omega t). \tag{1}$$

Here G is the total conductance of the active device, the circuit losses and the external load,

$$G = G_A + G_L + G_R \tag{2}$$

The complete solution for the voltage is

$$u(t)=\frac{A\omega_0}{G\omega_d}e^{-Gt/2C}\sin(\omega_d t)+\frac{A}{G}\sin(\omega_0 t) \tag{3}$$

with

$$\omega_d = \sqrt{\frac{1}{LC}-\left(\frac{G}{2C}\right)^2}, \qquad \alpha = \frac{G}{2C}, \ \omega = \omega_0 = 1/\sqrt{LC}. \tag{4}$$

The first term in (3) is the transient term that will grow or shrink exponentially, depending on the sign of the combined conductance G. The second term is the steady state voltage due to the driving current. If the combined conductance G gradually changes from a positive to a negative value, see Fig. 2, the transient term will soon dominate over the steady state term.

A stable oscillation with an angular frequency ω0 will occur when α=0. In reality, in a linear circuit, losses and gain never cancel out exactly. With some specific large signal nonlinear response of the conductance of the active device, GA, the combined conductance G will be negative within intervals of amplitude levels. This will permit the build-up of oscillations until a specific amplitude is reached. At this amplitude GA is equal, but with opposite sign, to GL+GR and a steady state limit cycle is created.

The bandwidth ωBW depends on the Q-value of the tank circuit when loaded,

$$\omega_{BW} = \frac{\omega_0}{Q}, \tag{5}$$

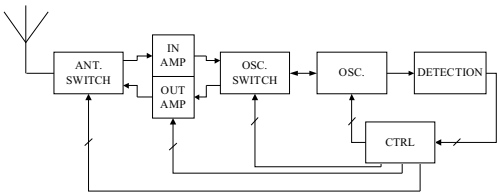

Fig. 3. Block diagram over a possible transceiver implementation.

where Q=1/(ω0 LG).

Properties such as energy consumption, sensitivity, and start-up time depend on the nonlinear parameter GA. Closed form expressions for these properties are thus hard to establish, if at all possible.

Energy will be consumed by the device supplying the negative conductance GA. This negative conductance may be realized by an NMOS transistor, exhibiting an increased negative conductance with increasing bias current. The figure of merit for the transistors in this case is transconductance efficiency, gm/ID. This can be found by the following expression for drain current in subthreshold operation [16]

$$I_{dsub} = \frac{g_m nkT}{q}, \tag{6}$$

where gm is the transconductance of the device, and n is the slope factor.

High efficiencies are found in subthreshold biased transistors, resulting in low power operation but also in large devices with large parasitic capacitances.

B. Circuit model

To simulate the proposed receiver in EDA software, we have developed a circuit model based on the basic detector model discussed above. A final radio most likely will operate one the 2.45 GHz ISM-band. We have chosen to make circuit models intended to operate at 24 MHz and 2.5 GHz. The relatively low frequency of 24 MHz gives us the possibility to evaluate and compare the response of the model with a simple discrete hardware prototype. If the receiver is to be realized in CMOS technology at GHz frequencies, the limited quality factor of available on-chip inductors at these frequencies will have an impact on power consumption. Using external inductors will, by their larger size, offer lower loss. A possible approach is to use the antenna as part of the resonance circuit, e.g. the antenna displaying an inductive loading to the circuit.

The realization of the receiver has been made as a sub-critically biased oscillator [14], Fig. 1b. The low frequency receiver consists of two matched NMOS transistors, in a differential oscillator topology. The high frequency receiver uses 180 nm line width NMOS transistors. The devices are biased to their subthreshold region, implying a weakly inverted channel. The negative conductance, GA, in the basic detector model is realized by the two cross-coupled NMOS devices. The admittance for this arrangement is

$$Y_A = G_A + jB_A = \\ = \frac{g_d - g_m + j\omega(C_{DS} + C_{GS} + 4C_{GD})}{2} \quad (7)$$

where gd is the output conductance of the transistor, and gm is the transconductance. The term CDS+CGS+4CGD/2 is the total parasitic capacitive load provided by the transistors, resulting in the reactive term BA.

The resistors R1 and R2 in the circuit model represent losses in the inductors and comprise part of GL in Fig. 1a. Capacitor C1 is a variable capacitive element added for tuning of the oscillator. In the circuit model we use a transformer, T1, for the inductive part of the tank circuit, and also for impedance matching to the interface of the measurement equipment impedance Z0. The incoming signal is represented by the current source iin. Detection of an input signal is made by monitoring the current driving the transistors, thereby using the rectifying function built into the circuit topology.

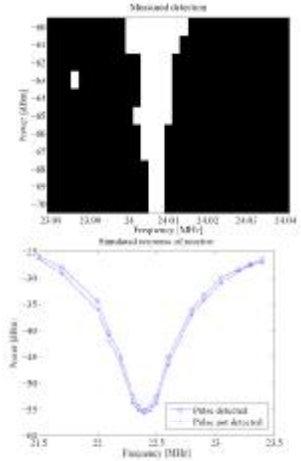

Fig. 4. Detection of incoming pulses at 24 MHz. Pulses with amplitude below the lower limit were not detected. Pulses with amplitude above the upper limit were detected. The isolated white dot in (b) is a false detection.

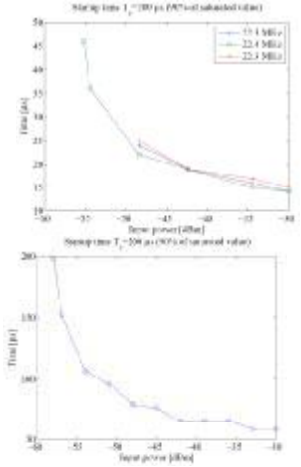

Fig. 5. Start-up time simulated (a) and measured (b), using excitation pulse duration of 200 μs.

1) Power consumption and Self calibration

The behavior of the circuit in Fig. 1a depends on the total conductive load G in (2). We are using MOS devices working in their subthreshold region, where there is an exponential dependence of transconductance to temperature. Keeping G as stable as possible is essential for the system; several strategies are possible, one suggestion being self calibration. This method has the potential to mitigate both fabrication and temperature variations. In Fig. 3 a proposed block schematic is found. The calibration can be performed as a binary process homing in on the bias point just below noise induced self oscillation, a similar method is described in [17].

False triggering may drain the power supply and must be minimised. Apart from using the above mentioned calibration strategies, this should also be handled at higher protocol level. As an example; we will use frequency hopping technique, where each hop has the potential to trig the receiver oscillations [13]. It follows that it is important to minimize the number of frequency hops used for addressing each single tag.

IV. Simulations and Measurements

A. Implementation at 24 MHz

The circuit model was implemented as a design network in EDA software, and its response to radio pulses was simulated with a time domain method. In the following we have used the detector as it stands in Fig. 1b. A hardware prototype was implemented with discrete components on a test board. Important properties such as sensitivity, bandwidth, start-up time and power consumption were investigated. The stimulation of the receiver was made by stepping three parameter values: bias voltage, radio signal frequency, and radio signal amplitude.

1) Sensitivity, bandwidth, and general frequency response

The hardware show a sensitivity better than -70 dBm and a bandwidth of 5 kHz or relative 0.02 percent, see Fig. 4b. The result of the corresponding simulations of the circuit model is a sensitivity of -45 dBm at 22.5 MHz, see Fig. 4a. The simple component simulation models used explain the significant discrepancy between simulation and measurement. The circuit model and the implemented circuit show a difference between idle mode sensitivity center frequency and final active mode oscillation frequency. This may be caused by the changed values of the dynamic element capacitors in the CMOS devices, but also by the change of the overall loss G in the circuit as we change the bias point of the devices.

2) Start-up time

The start-up time for the model and for the circuit implementation are found in Fig. 5a and Fig. 5b, respectively. The measurements and simulations were made with a 200 μs pulse length.

3) Biasing and power consumption

The sensitivity to biasing conditions is obvious in both measurements and simulations. The measurements show that

the circuit is fairly stable over time with a slight drift in the tens of millivolts range for the bias voltage keeping the circuit in state A.

The basic detector model predicts that the sensitivity bandwidth is controlled by the bias of the active element. This is also confirmed by measurements.

The power consumption was measured and simulated at the two operational states A and B of the receiver.

In state A we measured a current consumption of 64 μA and in state B the current was measured to 1.8 mA, with Vdd set to 1.6 V in both cases.

B. Implementation at 2.5 GHz

Foregoing an implementation of a transponder working at a higher ISM band a feasibility study was performed. The survey consists of researching a method for automatic calibration, and simulations and calculations of power consumption. Several combinations of circuit parameter values were tested. The channel width W of the transistors was varied between 700 μm and 175 μm, inductor value was varied between 0.651 nH and 2.604 nH, inductor Q-value was varied between 4 and 100, the interfacing impedance was varied between 50 Ω and 2000 Ω. Two implementations using transistor width W=175 μm have been studied in more detail. One implementation with interfacing impedance Z_0=2000 Ω and an inductor Q of 100, and one implementation with Z_0=500 Ω and a inductor Q of 25. To enable comparison the parameter values have been stepped through fixed values. This cause some spread in frequency of operation around the target of 2.5 GHz. Two simulation methods were used, linear frequency domain simulation, and time domain simulation.

1) Sensitivity, bandwidth, and general frequency response

Linear frequency domain simulation is fast but gives only an indication of the center frequency of the circuit. Further, it cannot be used to find the optimum bias point of the transistors in the detector. A difference in exhibited center frequency between linear frequency domain simulation and time domain simulation is noted. Linear frequency domain simulations of the circuits with Z_0=2000 Ω, Q=100 and Z_0=500 Ω, Q=25 show a center frequency of 2643 MHz with a 3dB-bandwidth of 0.8 MHz, and a center frequency of 2659 MHz with a 3dB-bandwidth of 1.4 MHz respectively.

To find the transconductance of the NMOS transistors in the linear frequency domain simulation a linear detector model was fitted to the detector model using transistors. A linear transistors model was composed by a conductance g_{lin} and three parasitic capacitors, gate to source capacitance C_{gs}, gate to drain capacitance C_{gd}, and drain to bulk capacitance C_{db}. The sensitivity center frequency achieved with time domain simulation for these component values are 2609 MHz and 2624 MHz respectively. The accuracy of the time domain simulations is limited to ±0.5 MHz by the cumbersome procedure of making one simulation for each pulse center frequency value. The final oscillation frequency (at steady state of oscillation) found with time domain simulation is 2444 Mhz and 2442 MHz respectively.

An overview of the results for the detector implementation using L=5.216 nH and transistors width W=175 μm is found in Table I.

All simulations have been made with the detector biased 1 mV below the level where self induced oscillation starts.

A matter of importance is the difference between final oscillation and the sensitivity center frequency of the detector. This will have an impact on how the detector may be used. If we want the detector to work as a backscatterer this difference must be incorporated in the communication protocol, otherwise the oscillation frequency has to be tuned during the transmitting period. In any case the current through the detector will increase and the incoming signal is detected.

2) Start-up time

The start-up time is dependent on the input power of the radio pulse in a non-linear way. Start-up times longer than 1 μs have been recorded as no detection.

3) Biasing and power consumption

The power consumption is lowest for the implementation with a combination of high impedance and high Q-value. Further, the lowest current and power is found with the largest inductor, which in turn gives the smallest transistor.

The total bias current I_d found in the simulations may be compared to the theoretically derived current through a subthreshold biased MOS transistor. With the transconductance values found with the linear model, g_m=0.606 mS and g_m=0.150 mS, we get I_{dsub}=30 μA and I_{dsub}=7.5 μA respectively. Which in turn gives us a total detector current of 60 μA and 15 μA, and a g_m/I_d of 20 using (6) with n=2. Such efficiencies have been reported, indicating that the present implementations are not running at their full potential [18]. The variation in power consumption is seen in Fig. 6.

V. CONCLUSION

In this paper we present a theoretical analysis and

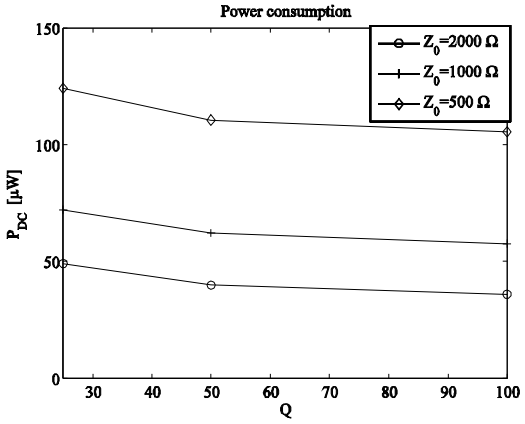

Fig. 6. Power consumption for the receiver in idle state. Implemented with L=5.216 nH and W=175 μm.

experimental verification of a novel radio receiver circuit suitable for low power application. We have built and

simulated a discrete 24 MHz design, and we have simulated a 2.5 GHz design.

We conclude that a bandwidth of 5 kHz at 24 MHz can be achieved at -70 dBm. This corresponds to a relative bandwidth of 0.02 percent and a Q-value of 5000.

The reason for discrepancies between measurements and simulations in sensitivity and current consumption may be found in the EDA-model of the transistor. The transistor model must correctly describe weak, moderate, and strong inversion of the channel, and also the transfer between those regimes.

The simple discrete implementation may be transferred to a monolithic design performing at higher frequencies, The relative bandwidth 0.02 percent is corresponding to 0.5 MHz at fc=2.5 GHz.

Simulations of a monolithic implementation using 180 nm CMOS transistors was performed around 2.5 GHz. In simulations the power consumption for the detector is below 125 µW at a sensitivity of -83 dBm and a bandwidth of 9 MHz.

The receiver has the potential to be used as a full transceiver by backscattering of the oscillations. In a final transponder implementation the antenna and the inductive part of the tank circuit may be placed outside the RFIC on the supporting structure.

TABLE I
SIMULATION RESULTS FOR DETECTORS IMPLEMENTED WITH L=5.216 NH AND W=175 MM OPERATING IN LISTENING MODE. ID IS TOTAL BIAS CURRENT. 2IDSUB IS THE TOTAL DRAIN CURRENT OF THE NMOS DEVICES FOUND BY USING (6)

Method	P_{sens} [dBm]	Z_0	Q	3 dB BW [MHz]	6 dB BW [MHz]	f_{sens} [MHz]	V_{dd} [V]	I_d [µA]	$2I_{dsub}$ [µa]
Frequency domain	-	500	25	0.8	1.4	2643	0.427	-	-
Time domain	-83	500	25	9	15	2609	0.427	291	60
Frequency domain	-	2000	100	1.4	2.4	2659	0.378	-	-
Time domain	-72	2000	100	13	17	2624	0.378	95	15

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