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A Low Power-Long Range Active RFID-system Consisting of Active RFID Backscatter Transponders

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***Abstract*—In this paper we present a novel active radio frequency identification system consisting of transponders with low complexity, low power consumption, and long system reading range. The transponder's low complexity and small circuit integration area indicate that the production cost is comparable to the one of a passive tag. The hardware keystone is the transponder's radio wake-up transceiver, which is a single oscillator with very low power consumption. The communication protocol, based on frequency signalling binary tree, contributes to the low complexity of the tag architecture. More than 1500 tags can be read per second. The average transponder ID read-out delay is 319 ms when there are 1000 transponders within reach of the interrogator. The calculated expected life time for a transponder is estimated to be almost three years.**

I. Introduction

THE emerging need for long range identifying systems indeed points out that the diversity in RFID technology need to be in focus. An interesting application for RFID is theft protection in stores and warehouses. There exist solutions, such as EAS transponders in combination with hard shells or Spider wraps. However, these solutions are believed to be too expensive, ineffective, and even having impact on sales. A global survey shows that shoplifting was seen as the major problem that retailers faced 2009, accounting for 42.5% of shrinkage, that is equivalent to $48.9 billion [1].

One drawback when using the Active RFID (A-RFID) techniques is that the transponder (tag) needs to be synchronized to the RFID-reader or listen continuously or periodically for the reader in order to know when it should deliver its identification number (ID). The active transponder needs an energy source of its own for this purpose. The active tag battery life time is then affected by how the synchronization is done. In this paper we describe a novel RFID system built on a frequency binary tree search protocol. The tag is using a wake-up radio technology, developed by Nilsson et al. [2], featuring very low power consumption when in sleep mode. Various solutions for wakeup adios have been published [3][4][5][6][7]. They suffer from difficulties like low receiving sensitivity resulting in short reading range, awakening due to false signaling, need of cyclic synchronizing, and need for a more complex transceiver. Our wake-up radio features high sensitivity, yielding a reading range of 50 meters, and a low complexity transceiver. The wake-up radio, also working as a transceiver, consists of a single LC-oscillator operated in the subthreshold region and thus exhibiting very low power consumption. This work shows a novel design of an RFID system based on tags using a small, low cost, mixed signal, mass produced ASIC. Such a low cost active-RFID tag could compete with passive-RFID tags in terms of price (typically a few cents). The same tag topology may also be used in a passive RFID system. A combined active/passive RFID system could thus be designed which utilizes readers with the capability of reading both active and passive tags. Using passive tags in some scenarios gives the added functionality of limiting the reading range to what is typical for passive RFID. An application where such tags may be of interest is in tagging medicine in order to counteract any attempts to use fake drugs in the medical field. Reports from the European Union state that counterfeit goods increased by 13% in 2008 with a 50% increase in fake medicines [8].

This paper is organized as follows; II) Short description of the hardware technology used in the transponder. III) Description of the communication protocol. IV) Description of the RFID reader. V) Performance of the system. VI) Conclusion. VII) Future work.

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II. Description of the Transponder

A. Principle of operation

An LC-oscillator, see Fig. 1, is used in the tags as a wakeup radio. The oscillator is designed to consume low power by operating in weak inversion region (subthreshold). The oscillator is biased near oscillation and a radio signal received by the antenna pushes the bias point into a region where stable oscillation is obtained. Fig. 2 illustrates how the RF-signal from the reader initiates the oscillation in the tag's wake-up radio receiver, resulting in a signal being transmitted back (backscattered) to the reader on the same frequency. The timing, TR, TT and Td, can be seen in Fig. 2. Idle state listed in Table I is when the oscillator is near oscillation and active state is when it is oscillating and transmitting.

There are two intended states of operation for the receiver, an idle state, where the receiver is armed and waiting for an input signal, and an active state, in which it has received an input signal and therefore is oscillating. The idle state corresponds to a bias point with lower gain, and the active state corresponds to a bias point with higher gain. The

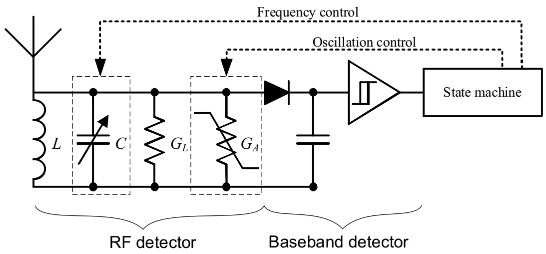

Fig. 1. Principle of the new wake-up radio transceiver architecture.

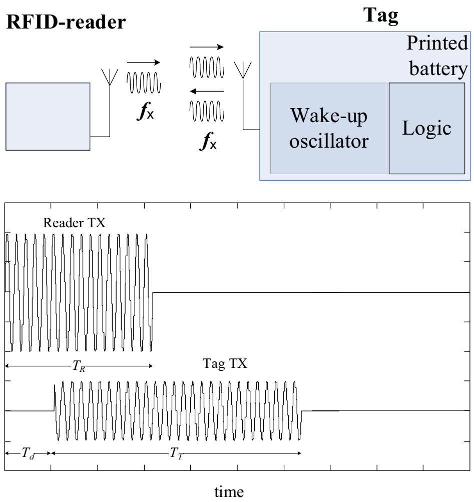

Fig. 2. Active backscatter. The timing diagram shows a reader transmitting (during time TR) and a tag responding (during time TT) on the frequency fx. The delay until the tag responds is the signal propagation delay, plus the start-up delay for the tag oscillator (during time Td).

nonlinear response is essential for the ability to achieve stability in each of the described states.

TABLE I
TRANSPONDER DATA.

Tag power consumption, idle state [mW]	0.02
Tag power consumption, active state [mW]	1.4
Tag sensitivity [dBm]	-72
Tag output power [dBm]	-10
Tag idle to active state [µs]	1.0

The nonlinearity is used for keeping the receiver at a stable equilibrium point when the input signal contains too little energy in the relevant frequency band. Out of band signals are discriminated by the tank circuit. When an input signal is applied, the average current of the oscillator is increased, following the path of the nonlinearity. The gain will be too small to form and sustain an oscillation to build up from noise at the bias point of the idle state. However, when the incoming pulse has sufficient energy, the effective bias is gradually pushed toward point active state, where an oscillation is created which sustains even when the exciting pulse vanishes. The necessary energy in the incoming pulse that may change state of the receiver depends on the nonlinear function of the active device, as well as on the Q-value of the tank circuit.

B. *Wake-up oscillator chip prototype*

A prototype oscillator is fabricated in UMC 180 nm CMOS technology and uses on-chip inductors. Simulations show that large energy consumption savings can be achieved (10 times lower) by instead using off chip inductors enabling much higher Q-value [2].The second version prototype will be using such off-chip coils (co-located with a printed battery [9][10]).

III. COMMUNICATION PROTOCOL

The protocol for communication between the tag and reader is described in [11] and is of the binary tree type [12][13][14], meaning that the ID is extracted bit by bit when traversing a binary tree detecting whether the tag's next ID-bit is a '0' or a '1'.

A. *Frequency coding, and allocation*

To extract bits in the tag ID, the protocol uses frequency signaling. The tags in the vicinity of the reader are first awakened by a beacon signal. The awakened tag's IDs are extracted by using four different frequencies, where every frequency corresponds to a two-bit combination in the ID as follows and is spread in the 2.45 GHz ISM band, see Fig. 3.

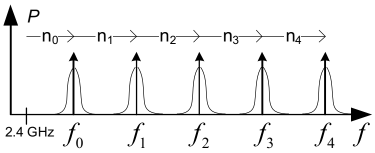

Fig. 3. Frequency spectrum allocation.

f_0: is the beacon signal, 2400+n_0 [MHz], used to wake up all tags in the reader's range
f_1: '00msb', 2400+n_0+n_1 [MHz]
f_2: '10msb', 2400+n_0+n_1+n_2 [MHz]
f_3: '01msb', 2400+n_0+n_1+n_2+n_3 [MHz]
f_4: '11msb', 2400+n_0+n_1+n_2+n_3+n_4 [MHz]

As an example of addressing a specific tag consider the following case

Tag ID = '10011100msb'.

To wake-up the tag with this ID (to see if it is available and to extract its information) the following sequence would be transmitted by the reader (sequence starts with a beacon, f0, to wake the tag, then specifying LSB→MSB),

$f_0, f_2, f_1, f_3, f_4, f_4, f_2, f_1,$

corresponding to the overlapping sequence of bit-pairs '10', '00', '01', etcetera.

B. Extracting the IDs of all unknown tags in the reader's range

It is possible to identify all tags in range for the reader without knowing anything in advance of the tag population. The ID extraction starts when the reader transmits the beacon signal (on frequency, f0), awakening all tags in reach. In the next step the reader transmits on all four frequencies, f1 – f4, simultaneously. A tag is initially "tuned" to the frequency corresponding to its two least significant ID bits, and the tag transmits back, only, when receiving a signal at its "tuned" frequency. This method is iterated, traversing bit by bit, halving the tag population until the there are only two bits left, the tags two most significant ID bits. When reading the two last bits in the ID, done in the final reading, there are two possible bit combinations left and two tags can be extracted at the same time.

C. Addressing a specific tag

In some applications it is known which tags that should be in vicinity of the reader. Instead of trying to read all tags it is possible to selectively read tags. If the ID of a tag is already known by the reader, then it is possible to address that specific tag. The reader uses the frequency "trail", which is composed of the bit combination in the tag ID, in a straightforward way. The addressing method is useful for saving tag energy, only doing a minimal number of activations of the tags.

D. Data transfer

It is also possible for the reader to retrieve information stored on the tag (e.g. sensor data). This is done by continuing the ID read cycle, but instead of retrieving ID bits from the tag, the reader retrieves the stored data.

IV. DESCRIPTION OF RFID READER

The RFID reader, depicted in Fig. 4, consists of the following blocks: RF/IF-converter, ADC, digital filter bank, and a controller unit. The digital filter bank and controller unit are hosted in a FPGA. In the input path the RF/IFconverter amplifies and mixes the RF-signal fRF down to the IF frequency f_{IF}. The down converted signal is filtered before it enters the FPGA circuit. The input power Pin to the ADC is kept to an optimum level by an Automatic Level Control (ALC) also providing the controller unit with a coarse value of the amplitude level. The output path of the converter consists of a four parallel synthesizers tuned to the decided output IF frequencies. The controller decides which of the synthesizers that should be active. Before the output signal is mixed up to fRF it is bandpass filtered by an analog filter. The RF frequency band of interest is set by tuning the LO synthesizer to the corresponding LO frequency fLO. Further optimization might be achieved by controlling the output power produced by the output Power Amplifier (PA).

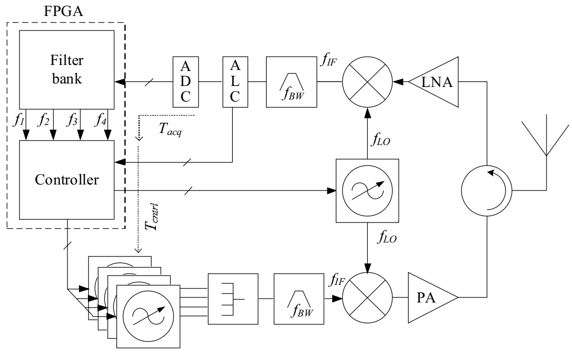

Fig. 4. Reader hardware implementation block diagram.

The ADC will have a bandwidth of $2f_{BW}$ using subsampling, or high speed sampling at $2f_{IF}$. The filter bank consists of four filters with a length of n_{FIR} bits. The ADC and the filter bank have available a period of T_{acq}, less than 4 µs, to sample the IF signal and to set the f_1 to f_4 signals indicating the presence of a signal above the noise floor at the specific frequencies. The controller and output signal synthesizer will have available a period of T_{cntrl}, less than 1 µs, to decide based on the protocol described in Section III, and to set the new appropriate vector of output signal frequencies. The synthesizers are in operation all the time eliminating the settling time for a new frequency. However, if not adding a fifth synthesizer, one of the four synthesizers has to be tuned to f_0 at the start of each new read sequence and then tuned back.

The FIR filters will work in sequence with the ADC, processing incoming ADC data, word by word. Thus the total sampling period T_p may be approximated to T_{acq} without any significant error. The limit filter frequency resolution is set by,

$$\Delta f = 1/T_{acq} \tag{1}$$

resulting in a resolution of 250 kHz. The minimum sampling frequency in MHz is,

$$f_s = 2f_{BW} = \sum_{0}^{4} n_i \,. \tag{2}$$

TABLE II

THE SYSTEM COMPONENT DATA.

Tag power consumption, idle state [mW]	0.02
Tag sensitivity [dBm]	-72
Tag output power [dBm]	-10
Reader sensitivity [dBm]	-85
Reader output power [dBm]	20

The required FIR filter length is $n_{FIR} = 2T_{acq}f_{BW}$.

The detection of a present signal is done by comparing the background noise power in the channel with the power received after an acquiring signal being sent. The noise is expected to be dominated by interferers rather than thermal noise when an LNA is used. The needed number of bits for the ADC will be established by this noise power and the expected signal power from the tags. The expected shifting noise level stress the need for an adaptive RF/IF converter. By using the ALC information the number of bits can be minimized.

The timing for the system can be seen in Fig. 5. When the reader is extracting a tag ID bit, it starts by transmitting a carrier at time t_0 on frequency f_x. Tag 1, which is assumed to have no propagation delay of the received signal, starts to build up oscillation immediately, and reaches stable oscillation at t_2. The delay due to propagation of the RF signal for tag N is assumed to be 170 ns (corresponds to max distance for the system, 50 meters), after which the tag starts to build up oscillation at t_1. At time t_4 the reader stops transmitting and starts to sense the radio channel; and continues to sense until t_5 and calculates an average value of the energy on the channel during this time. The reader then waits until t_7 so that every tag in the vicinity of the reader has stopped transmitting. The reader then, during $t_7 - t_8$, calculates an average of the energy when no tags are transmitting. By comparing the power levels at, sense 1 to sense 2 the reader is able to distinguish between tags answering and a noisy environment. A new bit extraction cycle starts at t_9.

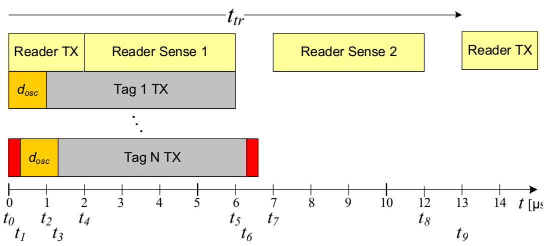

Fig. 5. Timing of the system when two tags are in reach of the reader. Tag 1 is close to the reader, tag 2 is at the rim of the area covered by the reader. ttr is the time needed to extract one bit from the tag ID.

A. *Low frequency prototype reader*

A reader prototype with a frequency range running from 20 MHz to 28 MHz, has been built and tested [15]. It is based on a 12-bit ADC and an FPGA. The filtering was implemented by using a fast Fourier transform (FFT) algorithm and by getting the power spectrum of the signal. The filter section was followed by a frequency identifier. The controller was implemented as a 100 MHz processor core on the FPGA. The length of each FFT output block was 512 bits giving a frequency resolution of 234 kHz. The FFT-block takes about 5 µs (derived by simulation) to complete one transformation, this means that during one listening cycle of 250 µs used in the prototype, 50 FFT calculations can be performed.

V. System Performance

The system performance is deduced from calculations and simulations in [11] and is presented as 1) readout delay, the time it takes in average to read a tag ID 2) the tag life time when draining the tag battery. 3) Operating range of the system. Calculations and simulations are based on numbers in Table II.

The average read-out delay with a population of 1000 tags is 319 ms. The maximum throughput is 1570 tags per second.

The calculated expected life time of how many days a battery will last if the reader tries to read the tags every 60 seconds is more than 900 days.

The range of the RFID system is calculated using the free space propagation loss formula

$$P_r = P_t \frac{G_t G_r \lambda^2}{(4\pi)^2 d^2 L} \qquad (3)$$

where P_r is the power available at the tag input port, P_t is reader output power, d is the distance, G_t and G_r is antenna gain set to 1, and L is system loss set to 1. Calculating both directions, reader to tag, and tag to reader, with values from Table II results in a maximum operating range of 50 meters, which fulfils the requirement for our A-RFID system.

VI. Conclusions

Wake-up radio technology, such as the one described and used in this paper, gives a number of benefits for RFID applications, most importantly that a tag is reachable by the RFID reader at anytime and does not need any advanced synchronized wake-up algorithms.

Like in conventional radio front-ends, important issues in wake-up radios are power consumption, method of synchronization, and total silicon area of the mixed signal die.

Reducing tag complexity infers a corresponding increase in reader complexity. In the low-frequency system that has been implemented and tested, the principle of operation has been proven. Transferring the design to the 2.45 GHz ISM band includes using standard off-the-shelf technology, with no added complexity or change in functionality.

The low complexity and power consumption of the described backscatter radio transceiver enables low-cost tags with long reading range, two-way communication (tag - reader), and sensor logging.

Synchronization between reader and tags is done using a frequency binary tree communication protocol that can be used for addressing single tags or for reading out all tags within reach from the reader.

With this active RFID system more than 1500 tags can be read per second. The average delay when reading a tag ID in a population of 1000 tags is 319 ms.

The reading range of this active RFID system is 50 meters. The estimated life time for a tag, in this active RFID system, powered by a low-cost 7x7 square centimeter printed battery, is almost three years, in a scenario where the tag's ID is read out as often as 60 times per hour.

VII. Future Work

The CMOS oscillator that is the foundation in the wakeup radio transceiver for the A-RFID tag is currently being refined. A digital architecture for running the protocol on the tag is under investigation and will be presented. The aim is to design an RFID system based on tags using a small, low cost, mixed signal, mass produced ASIC. Such a low cost active-RFID tag could compete with passive-RFID tags in terms of price.

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