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Low Noise Amplifier for Radio Telescope at 1.42 GHz

Master's Thesis in Electrical Engineering

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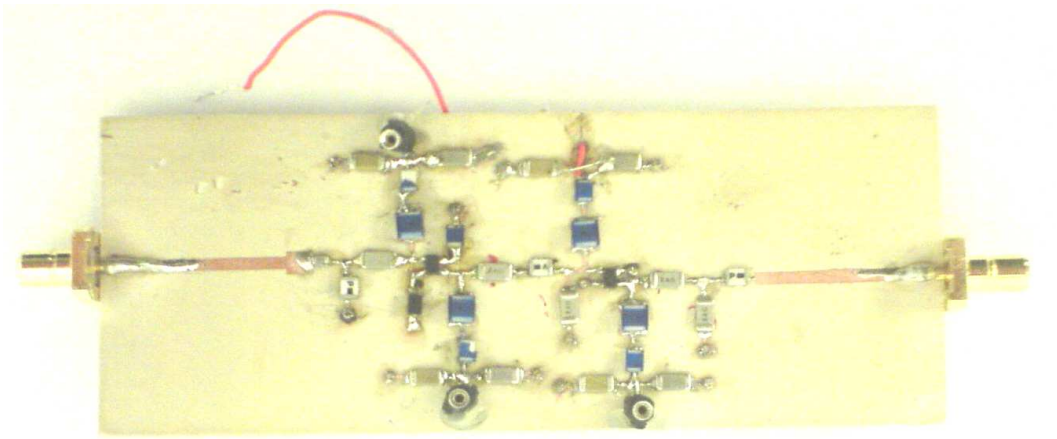

School of Information Science, Computer and Electrical Engineering

Halmstad University

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Halmstad University
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May, 2007

Description of cover page picture: low noise amplifier used for Radio telescope.

Preface

This Master's thesis in Electrical Engineering has been conducted at the School of Information Science, Computer and Electrical Engineering at Halmstad University. This is a part of the research project "Radio telescope system" working at 1.42 GHz. We realized that it would be hard to finish the project in time, but with all the kind help from the persons that are to be mentioned, we managed to carry the project to a conclusion within time. First of all we would like to thank Emil Nilsson and Professor Arne Sikö for providing us an opportunity to work on this project under their supervision and guiding us throughout the project. We would also like to thank Ruben Rydberg for his great help and advice throughout the project.

We are also very grateful to Jörgen Carlsson for his cooperation at every phase of our project. We would also like to give special thanks to Christopher Allen for correction, comments and proofreading of our thesis from an English point of view. Further, we are particularly very grateful to our parents who always supported and encouraged us during our stay and study in Sweden.

Venkat Ramana.Aitha & Mohammad Kawsar Imam
Halmstad University, May 2007.

Abstract

This is a part of the project “Radio telescope system” working at 1.42 GHz, which includes designing of patch antenna and LNA. The main objective of this thesis is to design a two stage low noise amplifier for a radio telescope system, working at the frequency 1.42 GHz. Finally our aim is to design a two stage LNA, match, connect and test together with patch antenna to reduce the system complexity and signal loss.

The requirements to design a two stage low noise amplifier (LNA) were well studied, topics including RF basic theory, layout and fabrication of RF circuits. A number of tools are available to design and simulate low noise amplifiers but our simulation work was done using advanced design system (ADS 2004 A).

The design process includes selection of a proper device, stability check of the device, biasing, designing of matching networks and layout of total design and fabrication. A lot of time has been spent on designing of impedance matching network, fabrication and testing of the design circuits and finally a two stage low noise amplifier (LNA) was designed. After the fabrication work, the circuits were tested by the spectrum analyzer in between 9 KHz to 25 GHz frequency range.

Finally the resulting noise figure 0.299 dB and gain 24.25 dB are obtained from the simulation. While measuring the values from the fabricated circuit board, we found that bias point is not stable due to self oscillations in the amplifier stages at lower frequencies like 149 MHz for first stage and 355 MHz for second stage.

Tables of Contents

1 Introduction……...1
1.1 Background ……...1
1.2 Purpose and Motivation…….2
1.3 Target Specification……..3
1.4 Outline of Thesis……...3

2 Related work……..5

3 Theoretical Background……...…7
3.1 Introduction of LNA…….…… 7
3.2 LNA Architectures…….....7
3.2.1 Resistive Termination……...……7
3.2.2 $1/g_m$ Termination……..9
3.2.3 Shunt Series Feedback …….9
3.2.4 Inductive Degeneration……10
3.3 RF Basic Concepts……10
3.3.1 Noise Figure…… 10
3.3.1.1 Noise Figure of Cascading Stages……11
3.3.2 Scattering Parameters…… 11
3.3.2.1 Definition of Scattering Parameters……12
3.3.3 Stability……14
3.3.3.1 Stability Techniques…….14
3.3.4 Transistor Biasing……14
3.3.4.1 Fixed Biasing ……..15
3.3.4.2 Collector to Base Bias …….16
3.3.4.3 Voltage Divider Bias ……...17
3.3.5 Smith Chart……...19
3.3.6 Impedance Matching……22
3.3.7 Gain……...26
3.3.7.1 Transducer Power Gain……...26
3.3.7.2 Operating Power Gain……26
3.3.7.3 Available Power Gain…….……....26
3.3.7.4 Maximum Unilateral Transducer Power Gain…… 27
3.3.7.5 Maximum Transducer Power Gain…….…… 27
3.3.7.6 Maximum Stability Gain…….…… 27

4 LNA Design Process……..…… 29
4.1Transistor Selection…… 29
4.2 Checking the Stability…… 29
4.3 Design a Biasing and Matching Networks..... 30
4.3.1 Simulation Result of two stage amplifier with ideal components……. 34

4.4 Layout of LNA……37
4.4.1 Simulation Result of Final Layout with real components……..38
4.5 Comparing Results……...41

5 Fabrication and Test plan ……...…… 43
5.1 Fabrication ……...…… 43
5.2 Test Plan……43

6 Conclusion and Future Work…… 47

7 Appendix ……. 49

8 Abbreviations……... 59

9 References...……..61

10 Permission……63

List of Figures

Figure 1	Block Diagram of a Typical Radio Receiver	2
Figure 2	Resistive Termination	8
Figure 3	$1/g_m$ Terminations	9
Figure 4	Shunt-series Feedback	9
Figure 5	Inductive Degeneration	10
Figure 6	Cascaded Noisy Stages	11
Figure 7	Two Port Networks	12
Figure 8	Fixed Bias	15
Figure 9	Collector to Base Bias	16
Figure 10	Voltage Divider Bias	17
Figure 11	Voltage Divider Circuits	18
Figure 12	The Smith Chart	19
Figure 13	Constant Resistance Circles	20
Figure 14	Constant Reactance Circles	20
Figure 15	Combination of Z and Y Smith Chart	21
Figure 16	Circuit	22
Figure 17	Power Graph	23
Figure 18	Showing the Basic Diagram of Matching Network for one Device	24
Figure 19 (a to d)	Examples of Matching Circuit	24 to 26
Figure 20	Stability Circuit with Ideal Components	30
Figure 21	DC Bias setup for Two Transistors	30
Figure 22	DC Bias Curves for Two Transistors	31
Figure 23	Bias Networks with Ideal Components for Two Stage LNA	32
Figure 24	Input Matching	32
Figure 25	Intermediate Matching	33
Figure 26	Output Matching	33
Figure 27	Total Matching Network for Two Stage LNA	34
Figure 28	LNA Simplified Schematic S-Parameters	34
Figure 29	LNA Simplified Schematic Stability Plot	35
Figure 30	LNA Simplified Schematic Noise Figure Plot	35
Figure 31	LNA Simplified Schematic Gain Plot	36
Figure 32	Final Schematic of LNA with Real Components	37
Figure 33	LNA Final Layout Schematic for Two Stage LNA	37
Figure 34	LNA Final Layouts	38
Figure 35	LNA Final Layout Schematic S-parameters	39
Figure 36	LNA Final Layout Schematic Stability Plot	39
Figure 37	LNA Final Layout Schematic Noise Figure	40
Figure 38	LNA Simplified Schematic Gain Plot	40
Figure 39	Fabricated Circuit	43
Figure 40	Bias Setup for a Single Transistor in First Stage	44

Figure 41	Bias Setup for a Single Transistor in Second Stage	45
Figure 42	Bias Setup for First Stage with Extra Feedback Resistor	45
Figure 43	Bias Setup for Second Stage with Extra Feedback Resistor	46
Figure 44	MSG / MAG and $\| S_{21} \|^2$ vs Frequency at 2 V, 10 mA	50
Figure 45	MSG / MAG and $\| S_{21} \|^2$ vs. Frequency at 2 V, 30 mA	52
Figure 46	V_{DS} vs I_{DS} Curve	52
Figure 47	Noise Figure Chart	52
Figure 48	Gain Chart	53
Figure (49 to 55)	Parts of Final Schematic	54 to 58

List of Tables

Table 1	LNA Architectures Results	3
Table 2	Compare Different Transistors	5
Table 3	K and Δ value from 1 GHz to 2 GHz	29
Table 4	DC Bias Point for Two Transistors	32
Table 5	Scattering Parameters of ATF 35143 Transistors (V_{DS} = 2 V, I_{DS} = 10 mA	47
Table 6	Typical Noise Parameters of ATF 35143	48
Table 7	Scattering Parameters of ATF 35143 Transistors (V_{DS} = 2 V, I_{DS} = 30 mA)	
Table 8	Typical Noise Parameters of ATF 35143 Transistors	49
Table 9	Typical Value of RO3003 Material	51

1

Introduction

1.1 Background

Radio astronomy deals the celestial objects in the universe by collecting and analyzing radio waves which are emitted by those objects **[1]**. The radio astronomers observe an entire range of celestial bodies consisting galaxies, planets, stars, pulsars and x-ray sources. The first identified astronomical radio source was invented by Karl Guthe Jansky in the early 1930's who is working as engineer in Bell Laboratories. By receiving and analyzing these radio emissions the scientists can extract the information about celestial bodies like its motion, size, composition, temperature, structure, evaluation and other properties. The radio waves emitting from celestial bodies are detected by specially arranged antennas, called Radio Telescopes.

Most of the material between stars is gas and it consists of individual atoms and molecules. The most abundant element in this gas is hydrogen and this neutral hydrogen will emits radio waves having a frequency 1420 MHz and a wavelength of 21 cm. These radio waves are used in radio astronomy to extract the information about amount and velocity of hydrogen in galaxy.

Neutral hydrogen consists of one proton and one electron and the orbital motion of the proton and electron also have spin. The spin of the electron and proton can be either parallel or anti-parallel because of magnetic interaction between the particles. If electron and proton aligned in same direction (parallel) will produce more energy than opposite direction (anti-parallel). When the hydrogen atoms switch from parallel to anti-parallel direction, they emit radio waves with a wavelength of 21 cm and a corresponding frequency of 1420 MHz. this is called 21 cm line. So a radio telescope tuned to this frequency is used to observe the great clouds of neutral hydrogen in the galaxy.

The first world's Radio Telescope was invented by Grote Reber in 1937. The majority of the radio telescopes use a parabolic reflecting antenna to receive radio emissions coming from the celestial bodies. The basic principle behind the Radio Telescope is that the incoming radio waves coming from the astronomical objects are reflected by the parabolic surface to produce an image at the focal point of the parabola. Then the signals are filtered, amplified and finally analyzed using computer. The sensitivity of the radio Telescope i.e., the ability to detect the weak signals coming from the radio emissions is depends on the area and efficiency of the antenna. And the sensitivity of the radio receiver is used to detect and amplify weak signals coming from the Radio sources

The function of any Radio System like Radio telescope **[2]**, Radar, Cellular Network, depends on the performance of the receiver, antennas and the propagation of radio waves between the source and destination. So the receiver is a key part in any Radio System and can be able to detect even weak signals among other strong signals. Therefore a high-quality receiver must have a good low

noise amplifier, mixer, IF amplifier and demodulator. The basic block diagram of radio receiver is as shown in below figure1;

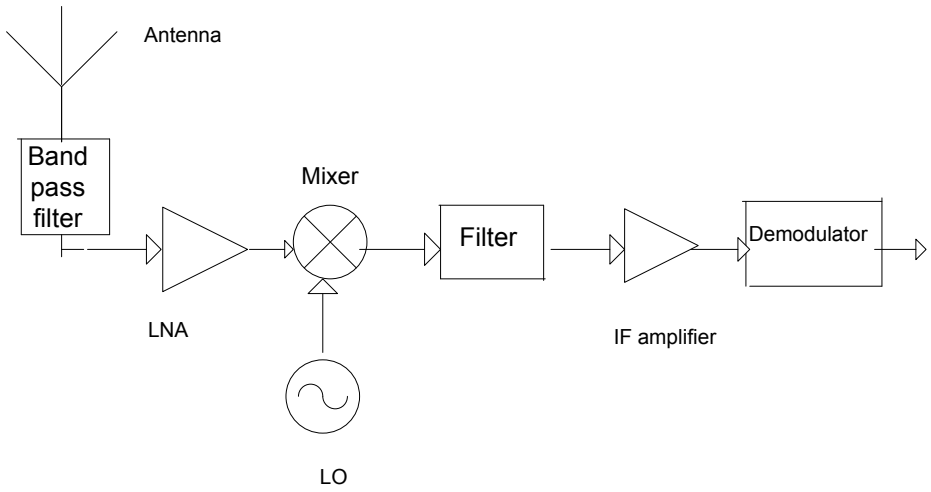

Figure 1 Block diagram of a Typical Radio Receiver **[2]**

Receivers are generally heterodyne or superhetrodyne in nature **[3]**, meaning that if an intermediate frequency coming from the mixer stage falls in audio frequency range, then it is called as heterodyne receivers. Similarly for IF frequency, if it falls in Radio frequency range it is called as superhetrodyne receiver. In the above block diagram an antenna will receive the signals from the space and feed to the next stage i.e**.** Low Noise Amplifier**,** which is an important part in receiver because the overall performance of the receiver depends on the characteristics of the low noise amplifier. So by designing a high-quality low noise amplifier we can design a good receiver.

Next the low noise amplifier (LNA) will amplify the received signals coming from the antenna to the detectable signal level and feed to the next stage i.e. IF amplifier, where it is again amplified and is finally given to demodulator section. At the end the demodulator recovers the original analog signal.

1.2 Purpose and Motivation

The Halmstad University, School of information science, Computer and Electrical Engineering, has an ongoing project on Radio astronomy. They require designing a patch antenna and a low noise amplifier working at 1.42 GHz frequency for their Radio Astronomy project.

A radio telescope system is used at this frequency, to measure the great clouds of neutral hydrogen found in the galaxy. To collect such radio waves at that particular frequency it needs one good receiving system, which includes parabolic dish antenna, patch antenna, LNA and mixer.

The main objective of this thesis is to design a two stage L-band LNA to extract a portion of our galaxy, which is full of hydrogen. Since most of the hydrogen in space emits radio waves at 1.42 GHz this is called as 21 cm line **[4]**. An advanced designing system (ADS 2004 A) tool is used to design and simulation of a two stage LNA as, first stage is for minimum noise figure and second stage for maximum gain. Finally this LNA is match, connect and test together with patch antenna to reduce the system components and signal loss.

1.3 Target Specifications

Parameters	**Specifications**
Operating frequency	1.42 GHz
Gain	$\geq$ 20 dB
Noise figure	$\leq$ 0.5 dB
Stability factor	Should be unconditionally stable
Bandwidth	More than 20 MHz

1.4 Outline of Thesis

Chapter 2- Related works
The information about related work in low noise amplifier (LNA) from past few years and compared proposed LNA to other research LNA is described in this chapter.

Chapter 3 Theoretical Background
Short description of RF Fundamental, LNA architecture, Introduction of LNA

Chapter 4 LNA Design Process
Describe a two stage LNA design process which includes transistor selection, checking the stability, design biasing and matching networks, amplifier layout, and total design and simulation results.

Chapter 5 Fabrication and Test plan
Fabrication process, component size, material and what type of components needs for testing the circuits is described in this chapter.

Chapter 6 Conclusion and Future work

2

Related work

This chapter discusses the most recent work on the LNA and the comparison between proposed LNA and other LNAs. Since past few years, the development of low noise amplifier (LNA) is increasing day by day in all communication systems. The low noise amplifier is most important block in any receiving system because the receiving system sensitivity is generally determined by its gain and noise figure. Most of the high frequency LNAs, such as L-band, X-band, Ku-band LNAs are designed in GaAs, CMOS, JFET, PHMET and MESFET technologies and are used in wide variety of applications like military aircraft, wireless communications, Radar communication, GPS applications and Radio astronomy. At the same time, low voltage, low power, ability to operate over a wide temperature range and better performances **[5]** are always the design targets, especially for designing LNA in Radio astronomy application.

There is wide range of options on designing an LNA; it can be either single ended or differential and it can also be single stage or multistage, depending on type of application and specifications. For every design options there are advantages and disadvantages. For instance the single ended architecture has one disadvantage that it is very sensitive to parasitic ground inductance. A differential LNA can solve this problem but with differential LNA, the noise figure is higher than single ended design option. **[5].** A multi stage LNA will provide higher gain but the problem is that it is difficult to maintain stability than single stage LNA. The trade-offs are not avoidable. The selection of design option depends on type of application and specific design goals.

In the literature, most of the LNAs are designed using inductive degeneration architecture. For every different frequency of operation and technology the load, stability, biasing and matching networks are slightly different. Also to reach better performance such as low power, low noise, high gain and more stability, there are more techniques available.

It is seen that there has been a change in trend towards designing a low noise amplifiers in last few years using CMOS, Bipolar, GaAs FET technologies. The table1 gives recent developments in low noise amplifier technologies and results during 1992 to 2006;

Author	NF (dB)	Gain (dB)	IP3 /-1 dB	Power (mW)	f_o (GHz)	Technology	year
Gramegna,G. **[6]**	1	13	-1.5	8.6	0.92	0.35 μm CMOS	2001
Gatta.F **[7]**	2	17.5	-6.5	N/A	0.9	0.35 μm CMOS	2001
Hung-Wei **[8]**	2.1	N/A	0.8	10	5	CMOS	2005

Guochi Huang **[9]**	0.47	20.5	18	11.8	2.14	CMOS	2006
Namsookim **[10]**	1.2	16.2	8	N/A	Low and High frequency	0.25 μm CMOS	2005
Adiseno **[11]**	4.6	18-26	1.5	36	0.9, 1.8, 2.4	CMOS LNA	2003
Weigo**[12]**	1.6	17.5	10.7	9	1.9	0.35 μm CMOS	2002
Benton et al **[13]**	2.7	28	N/A	208	1.6	GaAs FET	1992
Cioffi **[14]**	2.2	17.4	N/A	10	1.6	1 μm GaAs FET	1992
Imai et al. **[15]**	2.5	11.5	9 / N/A	14	1.6	0.3 μm GaAs FET	1994

Table 1 LNA Architectures Results

Where
N/A = Not applicable
CMOS =Complementary metal–oxide–semiconductor
NF= Noise figure
fo= Operating frequency

3

Theoretical Background

3.1 Introduction to LNA

Low noise amplifiers are the mainstay of radio frequency communication receivers and by knowing the specifications we can estimate the overall noise performance of the RF Receivers. An electrical device which is used to boost the desired signal power received at the front of communication system, while adding as little noise and distortion as possible is called Low Noise Amplifier.

LNA is placed as a first component of the receiving system. The noise figure of all the following stages in the receiving system is reduced by providing a low noise amplifier with high gain and low noise figure, thus it is very important for the low noise amplifier to amplify the received signal power by without introducing internal noise.

Low noise amplifiers are used in a wide variety of applications such as RF communication systems, cellular telephone, two way radio, personal digital assistant (PDA), personal computer (PC), and laptop computer with other communication systems. Low noise amplifiers are used in many systems where low-level signals must be sensed and amplified. Typically low noise amplifier used in communication transceiver for the amplification of weak electrical signals.

3.2 LNA Architecture

In the designing of low noise amplifiers, the important goals are minimizing the noise figure of the amplifier, **[16]** producing higher gain, low power consumption and producing stable 50 ohm input impedance. To achieve all these goals different LNA architectures are available. In following paragraph some of the LNA architectures are described.
There are four widely used LNA architectures; they are

- Resistive termination
- $1/g_m$ termination,
- Shunt series feedback
- Inductive degeneration.

Depending upon the requirements and the input impedance these can be simplified as follows, **[16]**

3.2.1 Resistive Termination

In resistive termination architecture**,** a resistor is added at the input side of the amplifier to get stable 50 ohm impedance, but will introduce some extra noise factor in the amplifier **[16]**. The effect of the termination resistor is explained as follows

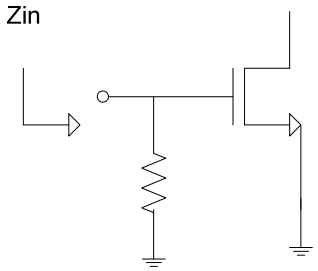

Figure 2 Resistive Termination **[16]**

$$F = \frac{\text{Total Output Noise}}{\text{Total Output Noise due to the source}}$$

The noise factor with termination resistor is given by following equation (3.1)

$$= 1 + \frac{Pna,i + kTBGa}{kTBGa} = 2 + \frac{Pna,i}{kTBGa} \quad \ldots\ldots\ldots (3.1)$$

Where

$P_{na,i}$ = Available noise power due to internal noise sources

B = Bandwidth over which the noise is measured

$G_{a\,=}$ Available power gain

K = Boltzmann's constant

T = Temperature

The noise factor without termination resistor is given by equation (3.2)

$$F = 1 + \frac{Pna,i}{4kTBGa} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3.2)$$

From the resulting equations we can see that by introducing a termination resistor the noise figure is increased by some percentage, The resistor noise which is added to the output, and the input attenuation makes the architecture unattractive resulting high penalty noise figure, for a more general situation wherein a good input termination is desired.

3.2.2 $1/g_m$ Termination

In this architecture, a source or emitter of common gate or common base configuration is used as the input termination **[16]**. This architecture produce lower noise factors compare to resistive termination.

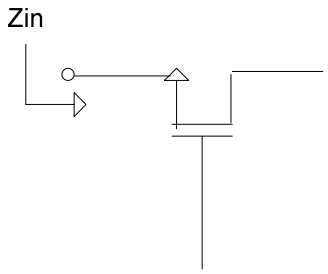

Figure 3 $1/g_m$ Terminations **[16]**

3.2.3 Shunt Series Feedback

This technique uses resistive shunt-series feedback **to** provide input and output impedance of low noise amplifier **[16]**. The amplifiers which use shunt-series feedback architecture will dissipate higher powers compare to other architectures along with similar noise performance.

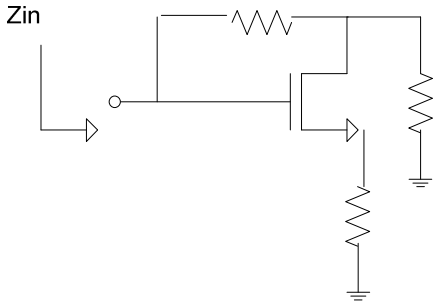

Figure 4 Shunt-series Feedback **[16]**

3.2.4 Inductive Degeneration

Inductive degeneration architecture is most commonly used in GaAs MESFET amplifiers. These amplifiers use inductive source or emitter degeneration to provide a real term in the impedance. This architecture provides **[16]** better noise factor than above mentioned architectures.
For our proposed low noise amplifier (LNA), Inductive Degeneration Architecture is used because of its low noise figure.

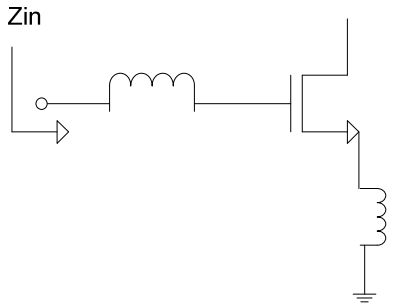

Figure 5 Inductive Degeneration **[16]**

3.3 Radio Frequency (RF) Basic Concepts

RF Theory is most important for designing any Radio Frequency (RF) circuits and there are many topics to discuss but basic Radio Frequency (RF) theory concepts will be discussed in this thesis for necessary understanding to design Radio Frequency (RF) amplifiers.

3.3.1 Noise Figure

Noise figure is commonly used to define extra noise generated by a circuit or system. It can also be said that, the ratio between **[17]** SNR at input to the SNR at output, and is expressed in decibels**.** It is expressed by following Equation

$$NF = 10\ log\frac{SNRin}{SNRout} \text{ in dB} \quad \text{..... (3.3)}$$

Where

NF= Noise figure

SNR_{in} = Signal to Noise ratio at the input of a circuit or system

SNR_{out} = Signal to Noise ratio of the circuit or system at output.

Or simply define by

$$NF = 10 \log \frac{\text{Total Output Noise Power}}{\text{Output Noise due to Input Source only}} \text{ in dB}$$

3.3.1.1 Noise Figure of Cascading Stages

In most cases the received signal strength **[18]** is very weak, and it is difficult to amplify the signal to the detectable signal level by using one amplifier. Therefore multi-stage amplifiers are used to accomplish this task.

Noise figure of the cascaded amplifiers can be calculated by Friis formula which is given in following Equation.

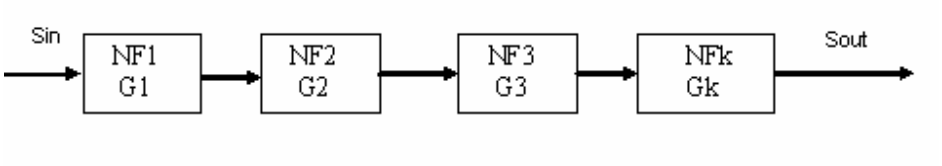

Figure 6 Cascaded Noisy Stages **[18]**

$$NF = NF_1 + \frac{NF_2 - 1}{G_1} + \ldots\ldots\ldots + \frac{NF_K - 1}{G_1 G_2 \ldots G_K} \ldots\ldots\ldots (3.4)$$

Where

NF = Noise figure

NF_1, NF_2 …NF_k = Noise figures of respecting stages in the system

G_1, G_2.....G_k = Gain of respected stages in the system.

3.3.2 Scattering Parameters

Scatter parameters are also called S-parameters **[19]**, and are related to the port parameters used in two port network theories. These parameters can be described by impedance (Z) and admittance (Y). At microwave frequencies S-parameters are very simple to measure. At high

frequencies, as compared to other kind of port parameters, S-parameters are simpler and provide detailed information about modeling problem.

S-parameters are defined in terms of the traveling waves which are scattered or reflected in the two port network when a circuit or network is connected to a transmission line with characteristic impedance Z_o.

3.3.2.1 Definition of S-parameters

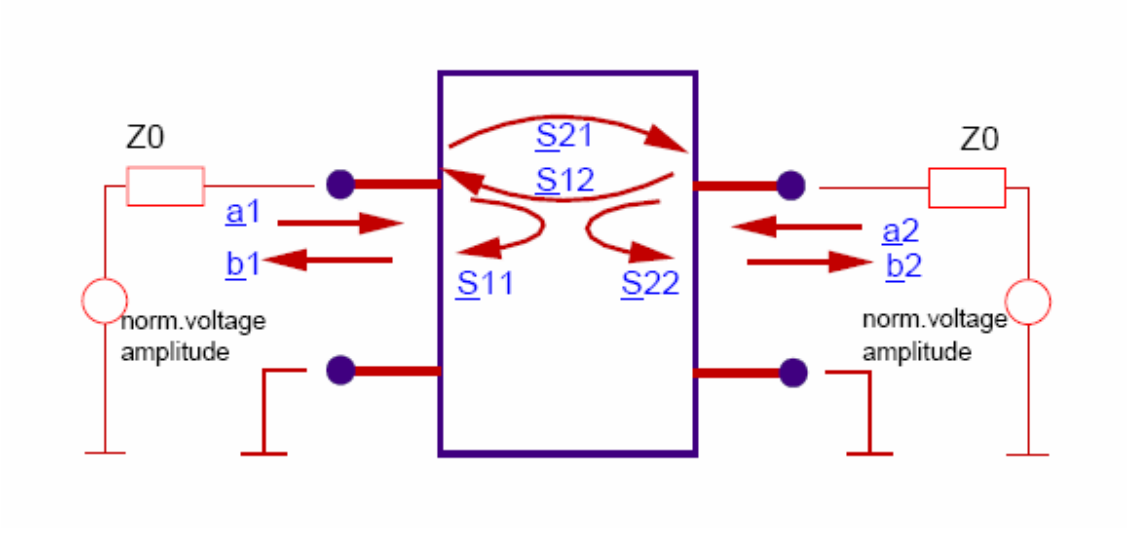

Figure 7 Two Port Networks **[19]**

The LNA is characterized **[19]** by the scattering matrix in Equation 3.5

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (3.5)$$

Where a_n represents the normalized incident voltage wave traveling towards the two-port network and b_n is the normalized Reflected voltage wave reflected back from the two-port network given by

$$a_1 = \frac{E_{i1}}{\sqrt{Z_0}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (3.6)$$

$$a_2 = \frac{E_{i1}}{\sqrt{Z_0}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (3.7)$$

$$b_1 = \frac{E_{r1}}{\sqrt{Z_0}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (3.8)$$

$$b_2 = \frac{E_{r2}}{\sqrt{Z_0}} \quad \text{..... (3.9)}$$

Where

E_i = Incident voltage wave measured in volts

E_r = Reflected voltage wave measured in volts

From the Equation 3.5, the parameters S_{11}, S_{12}, S_{21} and S_{22} which represent reflection and transmission coefficients, are called Scattering-parameters of the two port network and are measured at port 1 and port 2. The matrix for these parameters is;

$$S = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}$$

From Figure 7, The Scattering-parameters measured at the specific locations are defined as follows

$$S_{11} = \frac{b_1}{a_1} \text{ when } a_2 = 0 \quad \text{..... (3.10)}$$

$$S_{21} = \frac{b_2}{a_1} \text{ when } a_2 = 0 \quad \text{.....(3.11)}$$

$$S_{22} = \frac{b_2}{a_2} \text{ when } a_1 = 0 \quad \text{..... (3.12)}$$

$$S_{12} = \frac{b_1}{a_2} \text{ when } a_1 = 0 \quad \text{.....(3.13)}$$

Where

S_{11} = Input reflection coefficient

S_{22} = Output reflection coefficient

S_{12} = Reverse transmission gain

S_{21}= Forward transmission gain

a_1, a_2 = Normalized incident voltage wave traveling towards the two-port network

b_1, b_2 = Normalized Reflected voltage wave reflected back from the two-port network

3.3.3 Stability

Before going to start the design of low noise amplifier first the stability of the devices being used in the designing of LNA is checked. The stability of the Low Noise Amplifier or its tendency to oscillate at a range of frequencies is very important in any LNA design and can be calculated by using stability factor K and Δ **[19]**, which are given below

$$K = \frac{1+|\Delta|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{11}||S_{22}|} \quad \text{..... (3.14)}$$

and

$$\Delta = S_{11}^* S_{22} - S_{12}^* S_{21} \quad \text{..... (3.15)}$$

Where

S_{11} = Input reflection coefficient

S_{22} = Output reflection coefficient

S_{12} = Reverse transmission gain

S_{21}= Forward transmission gain

A device is unconditionally stable when K>1 and Δ<1. This characteristic means that the device does not oscillate over a range of frequencies with any combination of source and load impedance. If any amplifier satisfies any one of the conditions then the amplifier is said to be potentially stable amplifier. Unfortunately all the devices are not unconditionally stable. If any amplifier is not unconditionally stable it results the shifting of bias point or even destroy the transistor. But fortunately the designer can stabilize the amplifier by using some stabilizing techniques which are explained in the following section.

3.3.3.1 Stabilizing Techniques

By introducing some resistive **[19]** feedback at input side and resistive loading at output side, the designer can stabilize the amplifiers. Disadvantage to this technique is that it fails for designing low noise amplifier because the resistive terminations introduce some extra noise to the amplifier. In such cases the stabilization is done by providing inductors in emitter or source side, as the inductors are noiseless devices.

3.3.4 Transistor Biasing

Before applying an input signal to the amplifier quiescent point is needed to be set or bias point **[20]** at the middle of the load line. The process of setting the bias point at the middle of the DC load line by applying collector voltage and collector current is called Biasing .For every amplifier design, the designer can choose any of the following types of biasing circuits available.

- Fixed bias
- Collector to base bias
- Voltage divider bias

3.3.4.1 Fixed Bias

This is also called as base biasing method. In this method a base resistor **[20]** R_b is connected in between collector supply voltage and base of the transistor. But it is thermally unstable and causes Q-point variations, which results degradation of amplifier gain and noise figure.

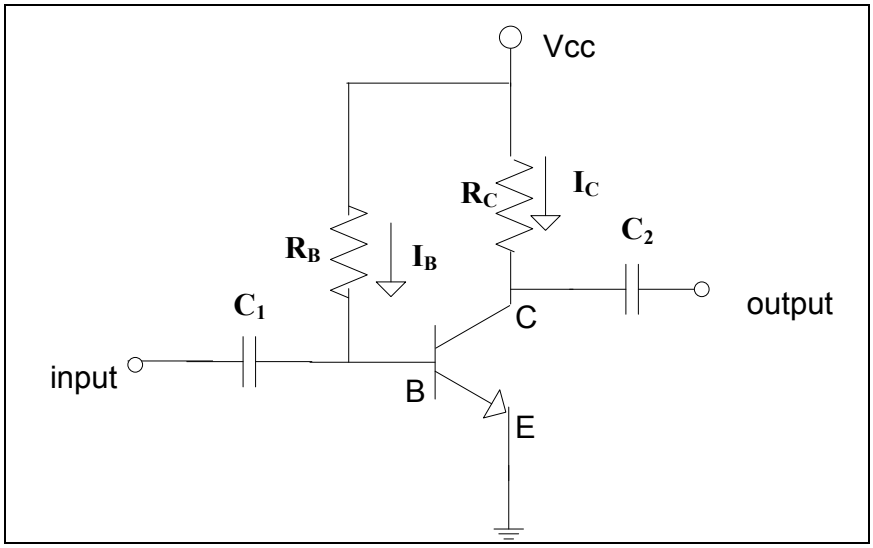

Figure 8 Fixed Bias **[20]**

Applying KVL in figure 8 and we can get

$$V_{CC} = I_B R_B + V_{BE}$$

Therefore $I_B = \frac{V_{CC} - V_{BE}}{R_B}$

Since $I_C = \beta_{DC} I_B$

$$I_C = \frac{\beta_{DC}(V_{CC} - V_{BE})}{R_B}$$

Again applying KVL $V_{CC} = I_C R_C + V_{CE}$

Therefore $V_{CE} = V_{CC} - I_C R_C$

Where
I_B= Base current
R_B=Base resistor
I_C= Collector current
R_C= Collector resistor
V_{CC}= Supply voltage
β_{DC}= Varies from device to device resulting in the variation of I_C
V_{BE}= Base to emitter voltage
V_{CE}=Collector to emitter voltage

3.3.4.2 Collector to Base Bias

This method is also referred to as self bias, in this method **[20]** a base resistor is connected directly between the collector and base of the transistor which provides forward bias. This arrangement is called self biasing. This self bias circuit overcomes thermal instability which is a problem in fixed biasing network.

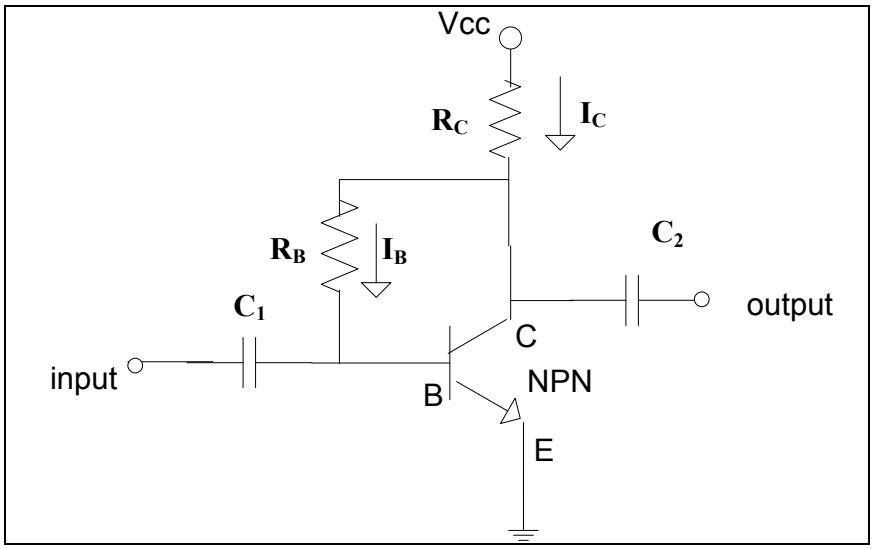

Figure 9 Collector to Base Bias **[20]**

We applying KVL in figure 9 and can write

$$V_{CC} = V_{RC} + V_{RB} + V_{BE}$$

$$= (I_C + I_B)R_C + I_B R_B + V_{BE}$$

$$= \beta_{DC} I_B R_C + I_B R_C + I_B R_B + V_{BE}$$

$$= (\beta_{DC} I_B + 1) I_B R_C + I_B R_B + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta_{DC} + 1)R_C}$$

$$V_{CQ} = V_{CC} - (I_{CQ} + I_B)R_C$$
$$\approx V_{CC} - I_{CQ}R_C \, when \beta_{DC} >> 1$$

3.3.4.3 Voltage Divider Bias

This is also called as Potential Divider Biasing. Among all of the above mentioned biasing techniques this is most widely used biasing technique because of the **[20]** greater operating point stability. But only the disadvantage is that it provides more noise figure due to more number of resistors.

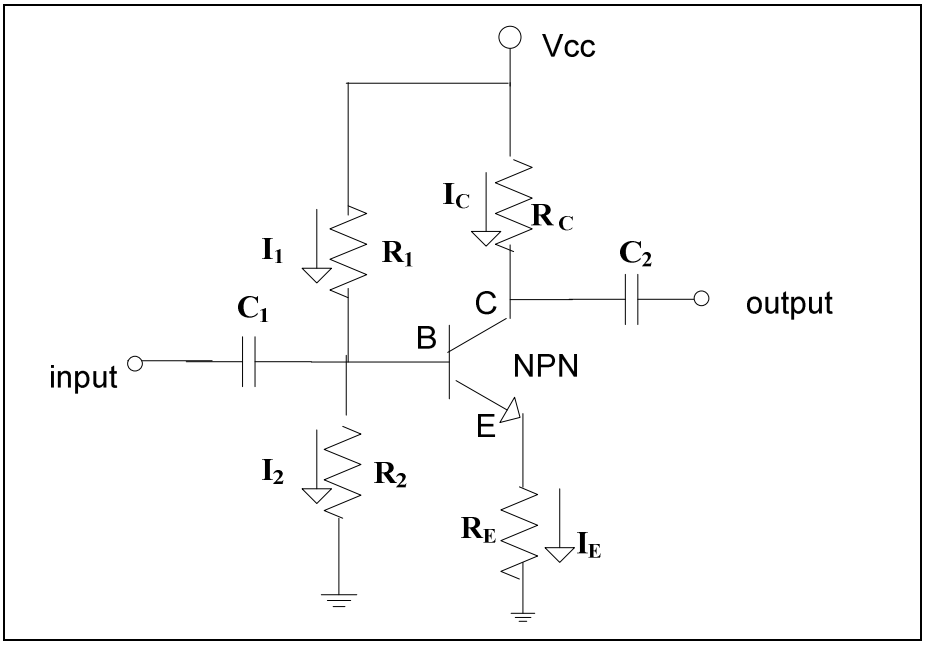

Figure10 Voltage Divider Bias **[20]**

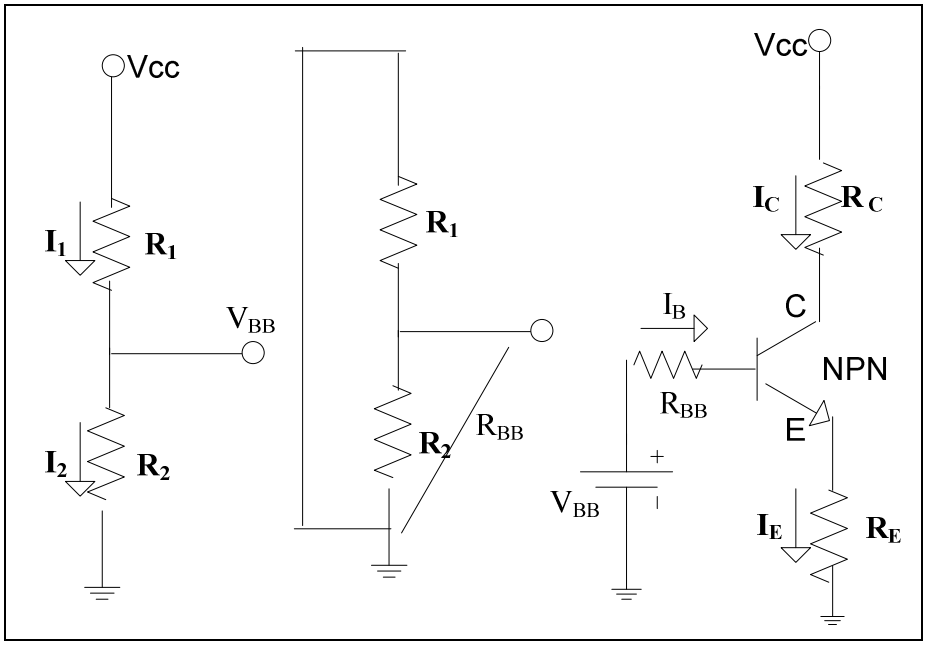

Figure 11 Voltage Divider Circuits **[20]**

From the figure 11, we apply KVL and can write

$$V_{BB} = \frac{R_1}{R_1 + R_2} V_{CC}$$

$$R_{BB} = \frac{R_1}{R_2}$$

$$V_{BB} = I_B R_{BB} + V_{BE} + I_E R_E$$

$$= I_B R_{BB} + V_{BE} + (\beta_{DC} + 1) I_B R_E$$

$$I_B = \frac{V_{BB} - V_{BE}}{R_{BB} + (\beta_{DC} + 1) R_E}$$

$$I_{CQ} = \frac{\beta_{DC}(V_{BB} - V_{BE})}{R_{BB} + (\beta_{DC} + 1) R_E}$$

$$V_{CEQ} = V_{CC} - (R_C + R_E) I_{CQ} when \beta_{DC} >> 1$$

3.3.5 Smith Chart

Most widely used graphical tool for RF designers to solve RF circuit problems is Smith chart. It was invented by Bell Laboratories Engineer Philip Smith in 1930's **[21]**, to solve any matching network which are mathematical solutions. It plays an important role in essential part of the process to easily see and estimate the range of possibilities in the line or load impedance application. It is easy to use and faster tool than most computer programs. The general smith chart diagram is given below

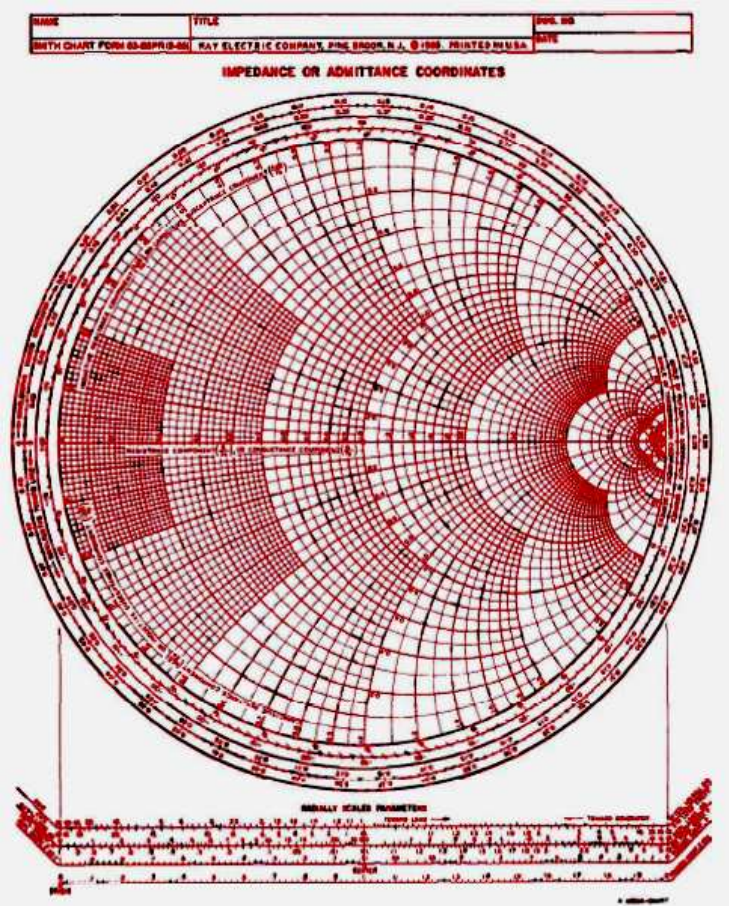

Figure12 The smith Chart **[21]**

By using above smith chart RF circuit problems including noise factor optimization, stability analysis and impedance matching circuits etc can be found. Among all the RF circuit problems above, designing of impedance matching circuits is very hard and important. The center point in Smith chart represents normalized impedance Z = 50 Ω which is the load in case of perfectly matched circuit. At the extreme left side of smith chart there is a point represents short circuit that means Z = 0 Ω and the in extreme right side there is one point which represents open circuit it means Z = ∞ Ω. Points elsewhere on unity circle represents pure resistance values and points on arcs will represents reactance values.

In impedance chart all circles are started from the right side. A large circle means decreasing resistance and it is noted as R. It does not matter where you are on the same circle; always resistance value is same on this circle. There is another reactance curve in the smith chart which starts from the right hand side and stretch out like increasing arcs is the reactance (jx).the bigger the arch is the smaller the reactance value.

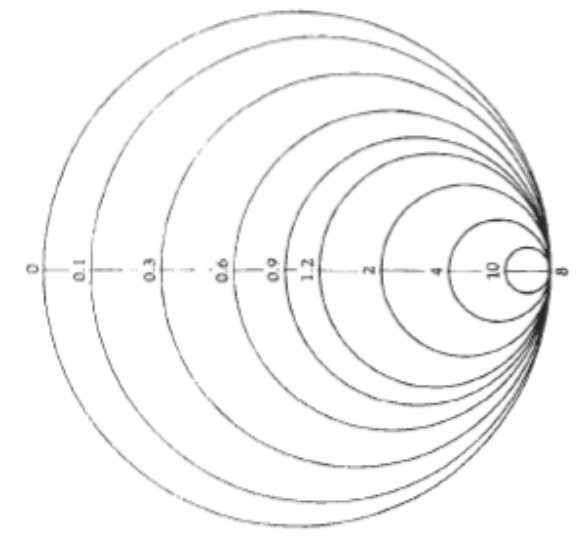

Figure 13 Constant Resistance Circles **[21]**

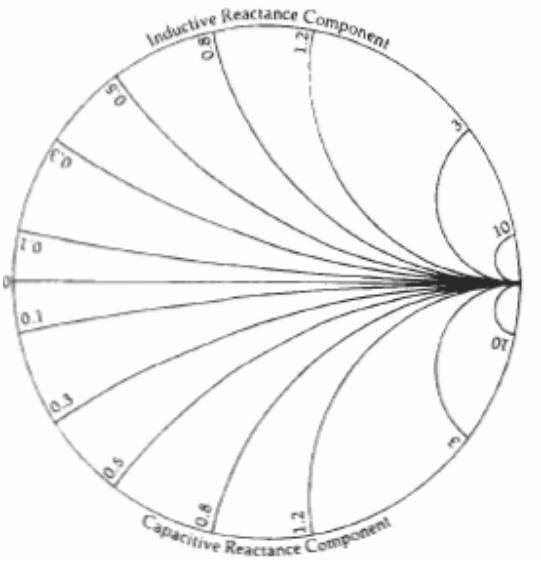

Figure 14 Constant Reactance Circles **[21]**

Along the horizontal line in the middle, the reactance is always zero because there is only resistive part. (R = 0).At this horizontal line end of the right side is open (R = ∞) and the left side circuit is shorted (R = 0).
Admittance chart (Y) is just like impedance. It is simply inverse of Z (Y = 1/Z) .graphically it is possible by rotating the smith chart 180^0 around. An impedance value can also be turned 180^0 around to find the admittance value. When both impedance and admittance chart shows in one figure than it is called normalized impedance and admittance coordinates smith chart. It is often referred to as a ZY smith chart. Figure 15 shows the combination of impedance and admittance smith chart.

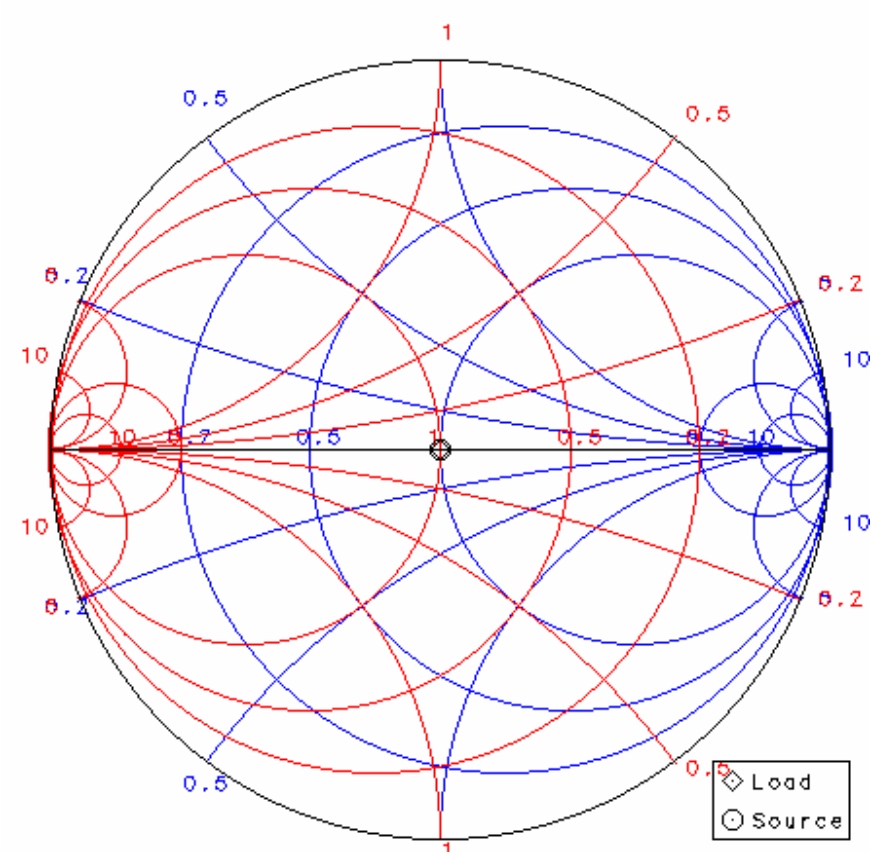

Figure 15 Combination of Z and Y Smith Chart **[21]**

Admittance chart contains both real and imaginary part same as impedance has Y = G ±jB
.
Where

G = Conductance

B = Susceptance

Many sources and loads have values greater than 50-ohm (Z_S = 50+j100, Z_L = 100+j100).The smith chart can not represent this value so the smith chart shows normalized impedance values. To transform to a normalized value first we have to know the characteristic impedance value Z_0 (50 Ohm, 75 Ohm) then simply divided the actual value of Z_S or Z_L with characteristic impedance Z_0 i.e. z = Z_S/Z_0 or z = Z_L/Z_0.

3.3.6 Impedance Matching

Impedance matching is an important and necessary in the design of RF circuits **[20]** in order to transfer the maximum power from source to its load. In front end of any sensitive receiver it is very important that there is such maximum power transfer, even if there is any loss in the circuit, carrying a weak signal levels cannot be tolerated. While designing such front end circuit's uttermost care has to be taken so that each device in the system is well matched to its load.

There is a well known theorem for DC circuits. Maximum Power Transfer theorem **[21]** states that a maximum power will be transferred from source to load when the load resistance R_L is equal to source resistance Rs. From Figure 16 it can be deducted that

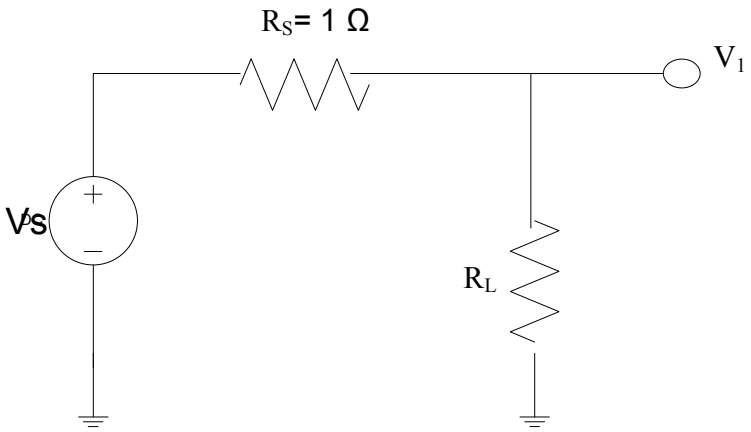

Figure 16 Circuit

$$V_1 = \frac{R_L}{R_S + R_L}(V_S) \quad \text{..... (3.16)}$$

Setting V_S =1 and R_S = 1 we get,

$$V_1 = \frac{R_L}{1 + R_L} \quad \text{.....(3.17)}$$

Then power into R_L is

$$P_1 = \frac{V_1^2}{R_L} \quad \text{..... (3.18)}$$

$$P_1 = \frac{\left(\frac{R_L}{1+R_L}\right)^2}{R_L} \quad \text{........ (3.19)}$$

$$P_1 = \frac{R_L}{(1+R_L)^2} \quad \text{..... (3.20)}$$

P_1 versus R_L plot is shown in Figure 17

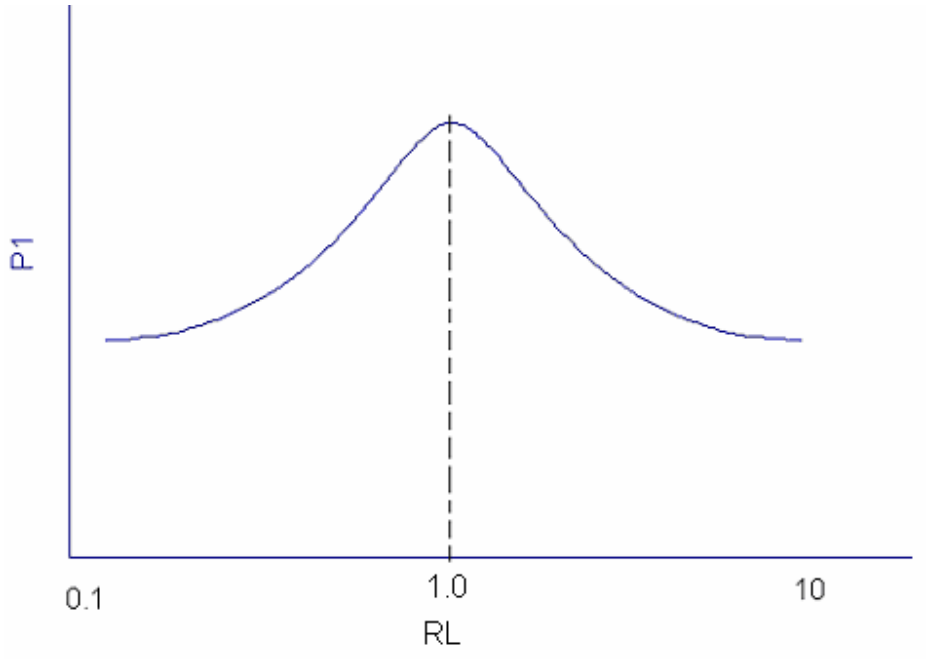

Figure 17 Power Graph **[21]**

For AC circuits the same theorem states that the maximum power will be transfer from source to its load when the load impedance Z_L equal to complex conjugate of source impedance Z_s.

The complex conjugate refers to complex impedance having the same real part with an opposite reactance. This is easier to show, if the source impedance is $Z_s = R+jX$ then its complex conjugate would be $Z_s = R-jX$

Figure 18 showing the basic block diagram of matching network for single stage amplifier

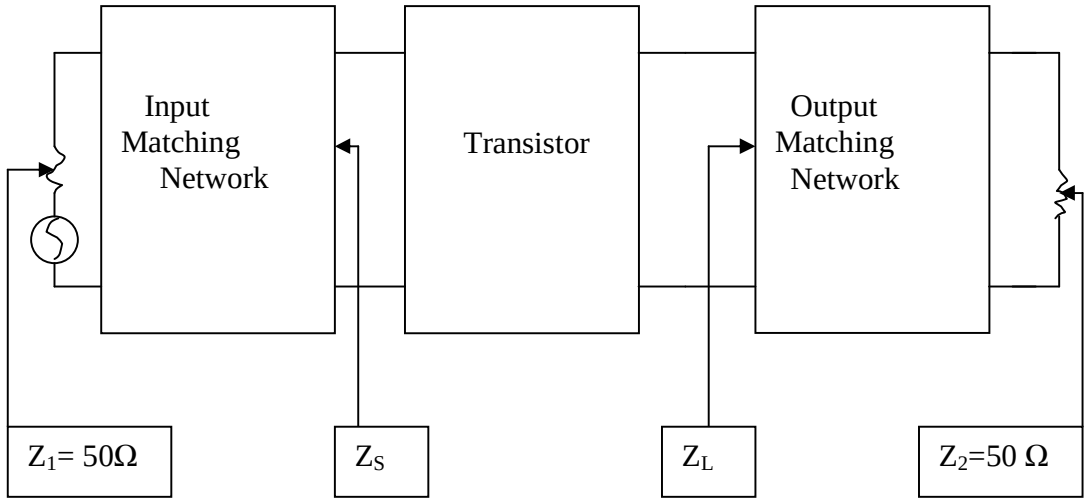

Figure 18 Showing the Basic Diagram of Matching Network for One Device **[21]**

There are many ways to implement matching networks sometimes using two element LC network or 7-element filter which depends on the type of application. To illustrate a two element LC network with an example, how an impedance match occurs between source and load, see the Figures from 19 (a) to 19 (d).

The first step is to determine the load impedance when the –j333 Ω capacitor is connected parallel to the 1000 Ω load resistor. Using Equation 3.21, the equivalent parallel impedance is calculated which is shown in Figure 19 (b). And finally to finish the impedance matching network, add calculated equivalent parallel impedance to the + j300 Ω which is shown in Figure 19 (c).Which causes + j300 Ω inductor and – j300 Ω capacitor to cancel each other resulting a 100 Ω load resistor value which is shown in Figure 19 (d).

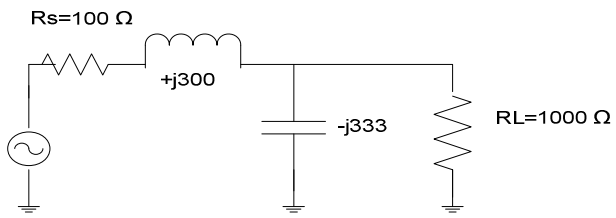

Figure 19 (a)

$$Z_X = \frac{X_C R_L}{X_C + R_L} = \text{100-j300} \text{ …..... (3.21)}$$

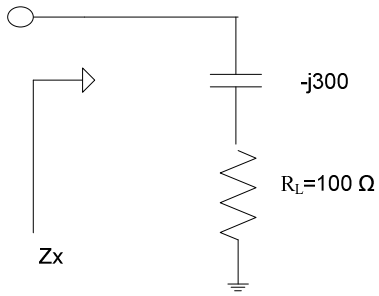

Figure 19 (b)

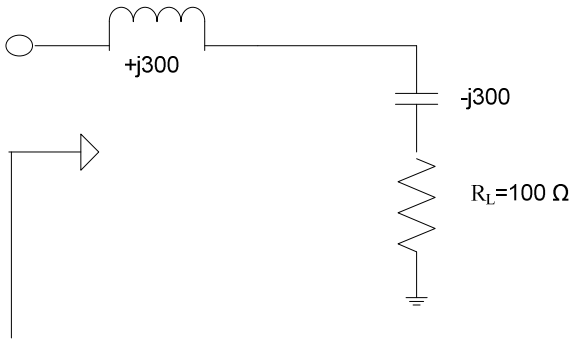

Figure 19 (c)

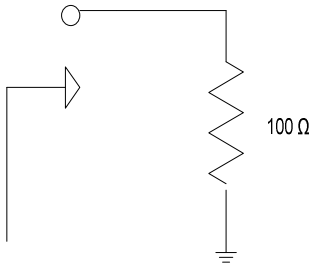

Figure 19 (d)

3.3.7 Gain

The ratio between the signal outputs of a system to signal input of a system is called gain. For LNA design there are three power gain definitions appears in the literature.

- Transducer power gain (G_T)
- Operating power gain (G_P)
- Available power gain (G_A)

3.3.7.1 Transducer Power Gain (G_T)

The ratio of the power **[22]** delivered to the load and the power available from the source is called Transducer power gain.

$$G_T = \frac{1-|\Gamma_s|^2}{|1-S_{11}\Gamma_s|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-\Gamma_{out}\Gamma_L|^2} \quad \text{..... (3.22)}$$

3.3.7.2 Operating Power Gain (G_P)

The ratio between powers **[22]** delivered to the load and the power input to the network is called Operational Power Gain.

$$G_P = \frac{1}{1-|\Gamma_{in}|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \text{ ..... (3.23)}$$

3.3.7.3 Available Power Gain (G_A)

The ratio between the power available **[22]** from the network and power from the source is called Available Power Gain.

$$G_A = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}|S_{21}|^2 \frac{1}{1-|\Gamma_{out}|^2} \quad \text{..... (3.24)}$$

Beside these three gain definitions, there are three additional gain definitions that can be use for LNA design.

- Maximum unilateral transducer power gain (G_{umx})
- Maximum transducer power gain (G_{max})
- Maximum stability gain (G_{msg})

3.3.7.4 Maximum Unilateral Transducer Power Gain (G_{umx})

G_{umx} is the transducer power gain with assumption **[22]** of S_{12} to be zero and the source- load impedances are conjugate matched to the LNA, i.e. $\Gamma s = S^*_{11}$ and $\Gamma_L = S^*_{12}$.

$$G_{umx} = \frac{1}{|1-|S_{11}|^2|}|S_{21}|^2 \frac{1}{|1-|S_{22}|^2|} \quad \text{..... (3.25)}$$

3.3.7.5 Maximum Transducer Power Gain (G_{max})

G_{max} is the simultaneous conjugate matching power gain **[22]**, when input and output both are conjugate matched.$\Gamma_S = \Gamma^*$in and $\Gamma_L = \Gamma^*$out when S_{12} is small and G_{umx} is close to G_{max}.

$$G_{max} = \frac{|S_{21}|}{|S_{12}|}\left(K - \sqrt{K^2-1}\right) \quad \text{..... (3.26)}$$

Where
K= Stability

3.3.7.6 Maximum Stability Gain (G_{msg})

G_{msg} is the maximum of G_{max} when stability k **[22]** is greater than one is still satisfied.

$$G_{msg} = \frac{|S_{21}|}{|S_{12}|} \quad \text{.....(3.27)}$$

4

LNA Design Process

Low noise figure and gain are the most critical points in designing an LNA at single frequency. That is the reason there are many different designs proposed in past. Here, below, a design is proposed for two stages LNA at 1.42 GHz frequency. For LNA design there are some steps followed and all the figures and tables in this chapter are taken from simulation results of our designed LNA using Advanced Design System (ADS) Software.

4.1 Transistor Selection

This is one of the most important steps in designing a low noise amplifier (LNA). Different types of transistors are available, for example, MESFET, HEMT and PHEMT which can be used for LNA application. According to our specifications, GaAs PHEMT transistor has been used for two stage low noise amplifier due to its low noise figure and high gain. Table 2 shows three different types of transistors and specifications of these transistors at 2 GHz frequency **[24]**.

Part No	Gate width	Bias point	Noise Figure (dB)	Gain (dB)
ATF-33143	1600 µ	4 V, 80 mA	0.5	15.0
ATF-34143	800 µ	4 V, 60 mA	0.5	17.5
ATF-35143	400 µ	2 V, 10 mA	0.4	18.0

Table 2: Compare Different Transistors **[24]**

Out of the three transistors from table 2, Agilent ATF-35143 PHEMT transistor is chosen for two stage low noise amplifier (LNA), and datasheet for this transistor was downloaded from Avagotech website and is included in appendix section. Agilent's ATF-35143 being small in size gives low noise and support wide range of frequencies (450 MHZ to 10 GHz) and also it is a surface mount plastic package, good for future use **[24]**.

4.2 Checking the Stability

Before designing any low noise amplifier (LNA) every designer has to check the stability of the device chosen for design. Manually, the calculations are very long but it is much quicker to simulate in any circuit simulating tool, for this ADS simulator was used to check the stability of the device and it was found that the selected ATF 35143 is potentially stable to the desired frequency at 1.42 GHz. To stabilize at frequency range between 1 GHz to 1.98 GHz. one inductor value 1.8 nH was added to the source side of the first transistor. The Figure 20 and Table 3 show the stability of the device over a range from 1 GHz to 2 GHz frequencies.

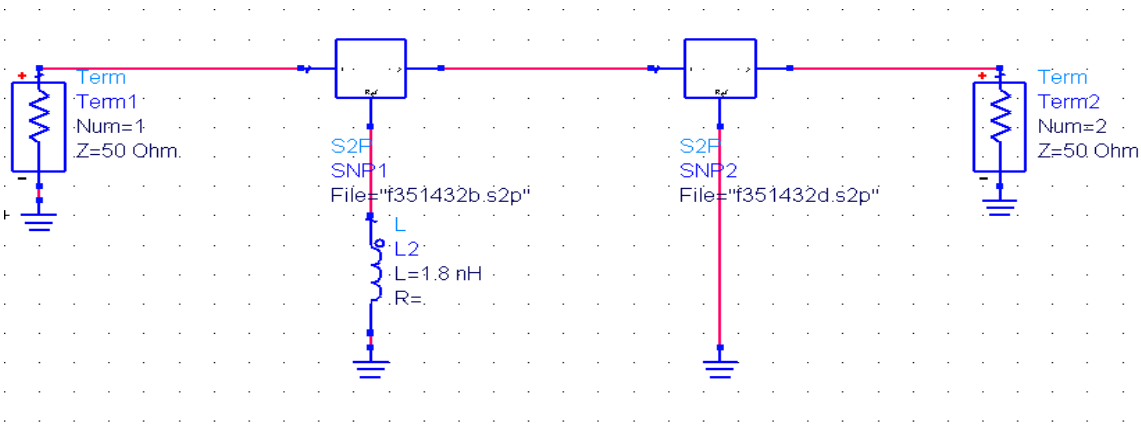

Figure 20 Stability Circuit with Ideal Components

Frequency (GHz)	K	Δ
1.000	2.746	0.106
1.140	2.820	0.080
1.280	2.881	0.061
1.420	2.928	0.048
1.560	2.980	0.039
1.700	3.044	0.036
1.840	3.088	0.036
1.980	3.112	0.038

Table 3 K and Δ value from 1 GHz to 2 GHz

4.3 Design a Biasing and Matching Networks

The next step is to check the DC bias point of two transistors and to design corresponding biasing networks. For the desired application bias points (Vds = 2 V, Ids=10 mA) are chosen for first transistor and (Vds =2 V, Ids = 30 mA) for second transistor .The Figure 21, Figure 22, Figure 23 and Table 4 below show the dc bias set up for two transistors and the corresponding results.

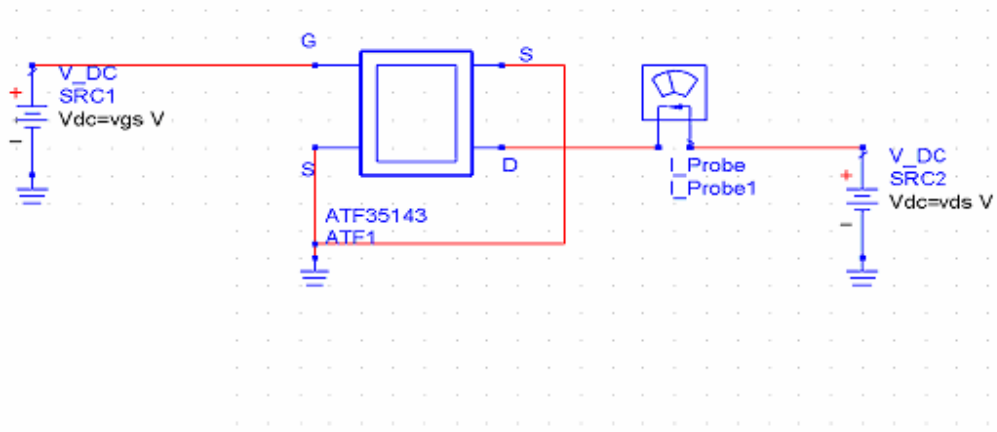

Figure 21 DC Bias Set Up for Two Transistors

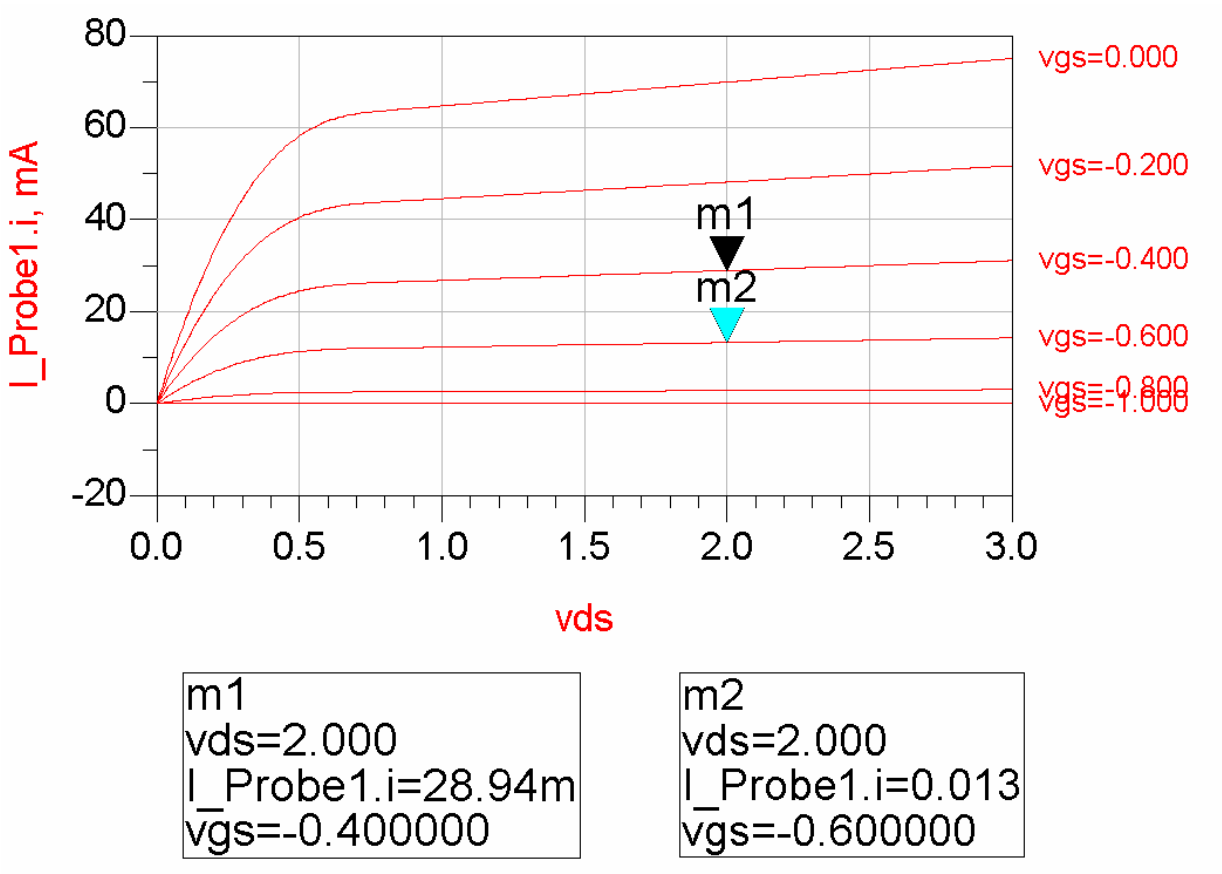

Figure 22 DC Bias Curves for Two Transistors

First stage	Second stage
Vds = 2 V	Vds =2 V
Vgs = -0.65 V	Vgs = -0.39 V
Ids =10 mA	Ids =30 mA

Table 4 DC Bias Point for Two Transistors

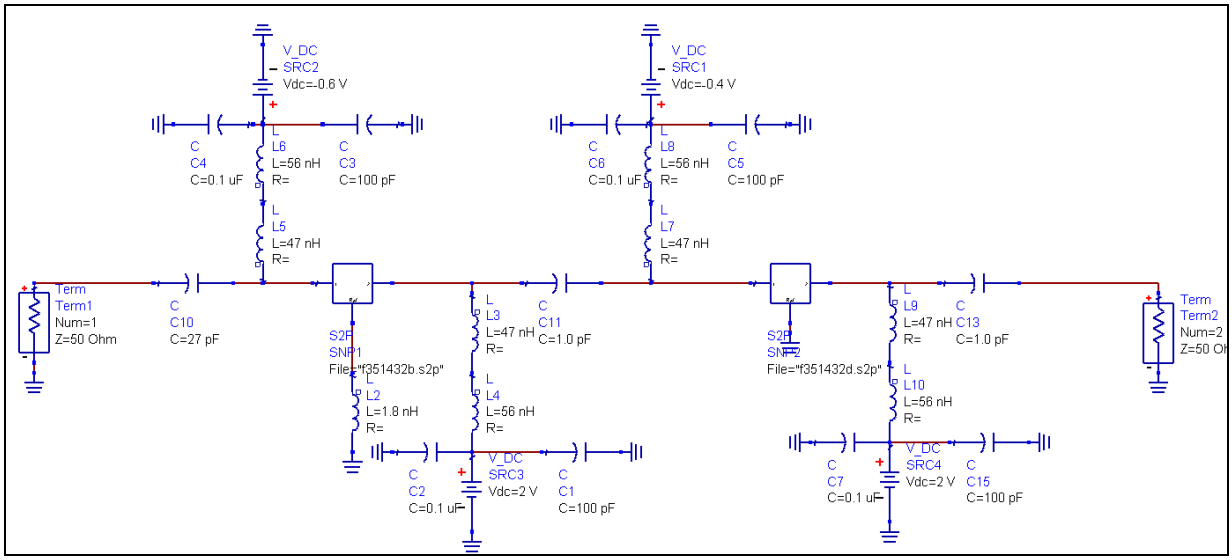

Figure 23 Bias Networks with Ideal Components for Two Stage LNA

Next step after designing biasing networks for two transistors was to build matching circuits for two stages low noise amplifier (LNA). To design such matching networks smith chart was used from ADS software. The following Figure 24 to Figure 27 show the input, intermediate, output and total matching circuit for two stage LNA.

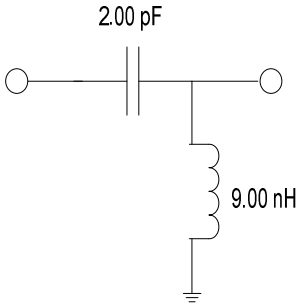

Figure 24 Input Matching

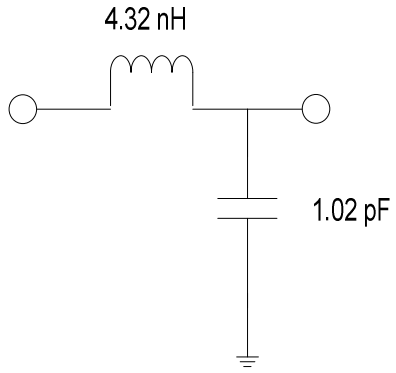

Figure 25 Intermediate Matching

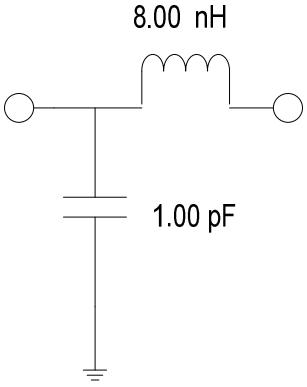

Figure 26 Output Matching

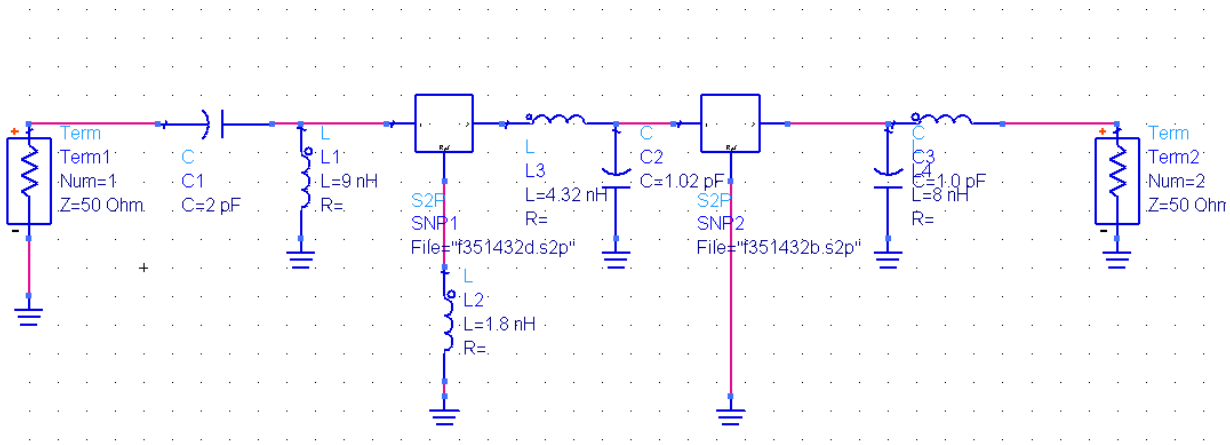

Figure 27 Total Matching Network for Two Stage LNA

Utilizing the ideal components provided by the use of an ADS software component pallet, a two stage low noise amplifier design was proposed. Ideal components cannot be used for layout and fabrication of LNA with respect to real components. The process of amplifier layout and fabrication will be explained in layout and fabrication sections.

4.3.1 Simulation Results of Two Stage Low Noise Amplifier with Ideal Components

In this section simulated results of noise figure, scattering parameters, gain, and stability chart of proposed LNA design are showing

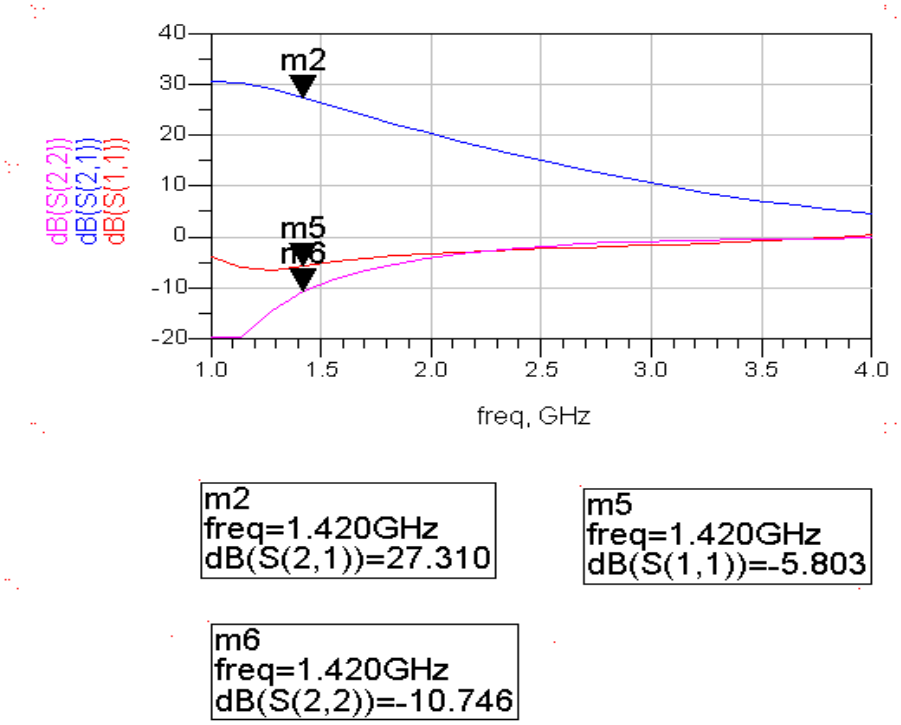

Figure 28 LNA Simplified Schematic S-Parameters

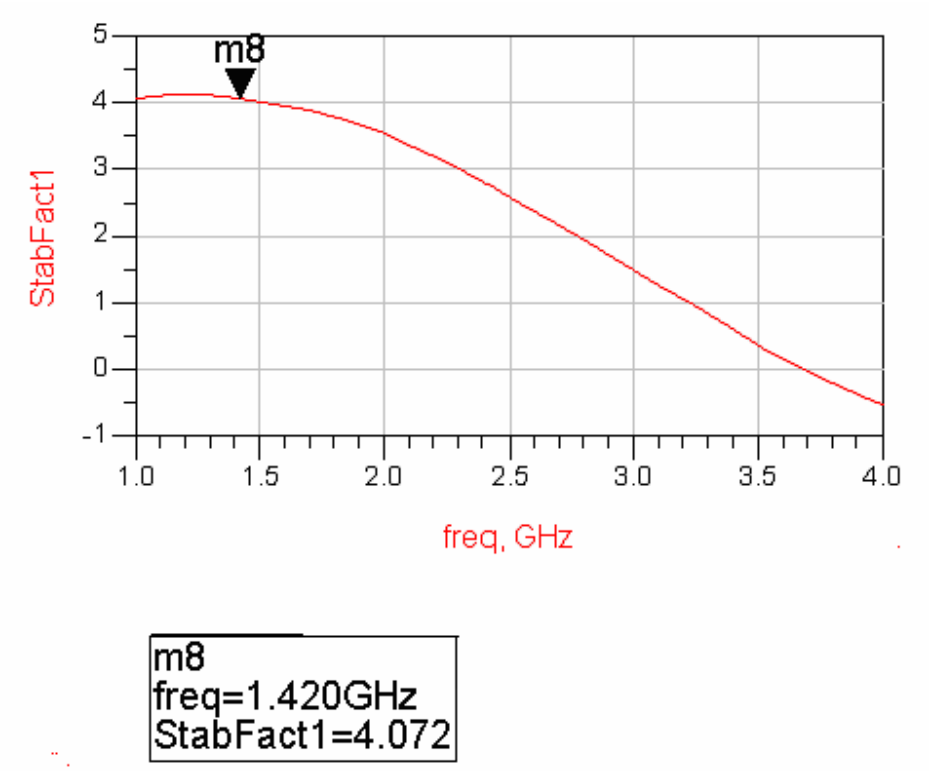

Figure 29 LNA Simplified Schematic Stability Plot

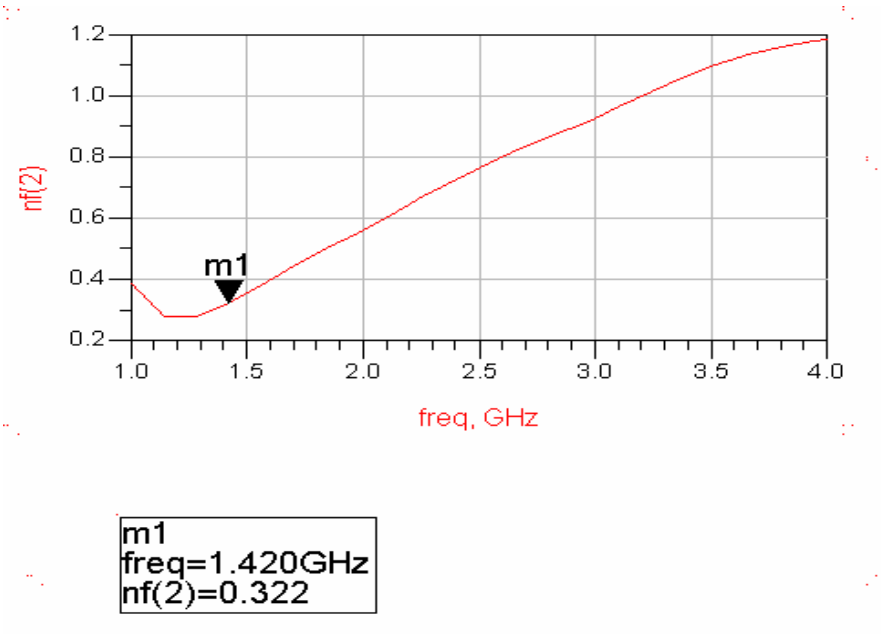

Figure 30 LNA Simplified Schematic Noise Figure Plot

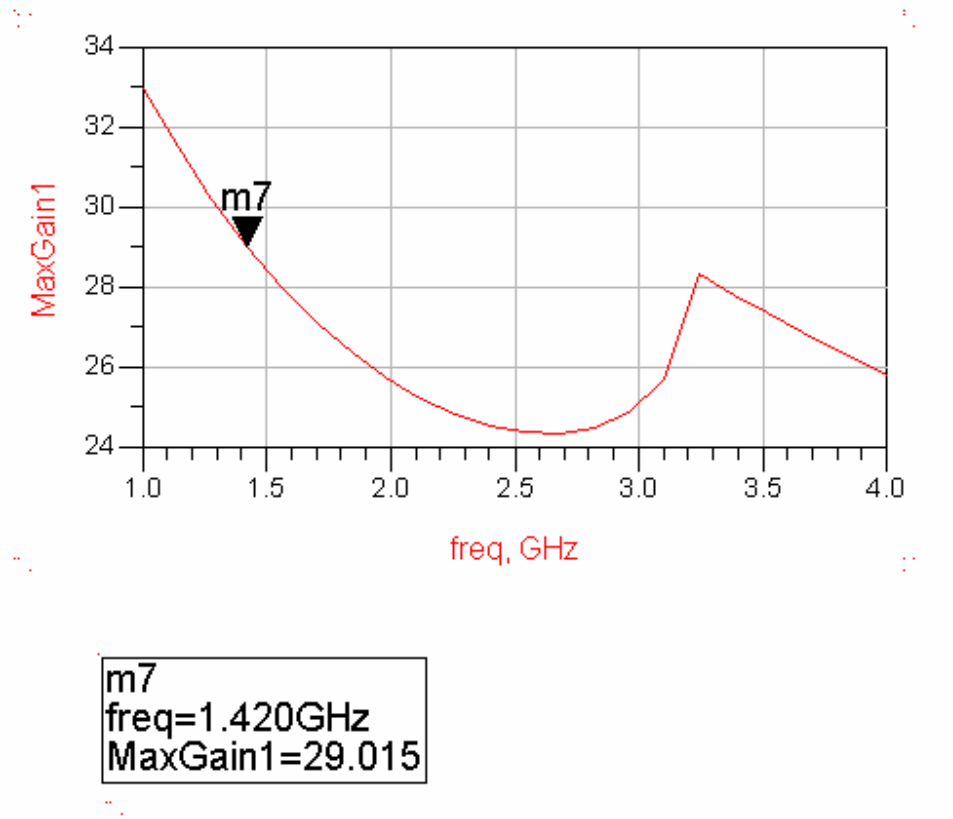

Figure 31 LNA Simplified Schematic Gain Plot

4.4 Layout of LNA

To make a layout for any RF circuits the designer needs a real component foot prints. For this task, design kit from Murata manufacturers was downloaded which includes all the real components. Finally ideal components of two stages LNA were replaced with real components and a layout using ADS software. Figure 32 to Figure 34 below shows the final layout of LNA schematic with ideal and real components and layout. The Figure 33 is divided into several parts and it is showing in the appendix section.

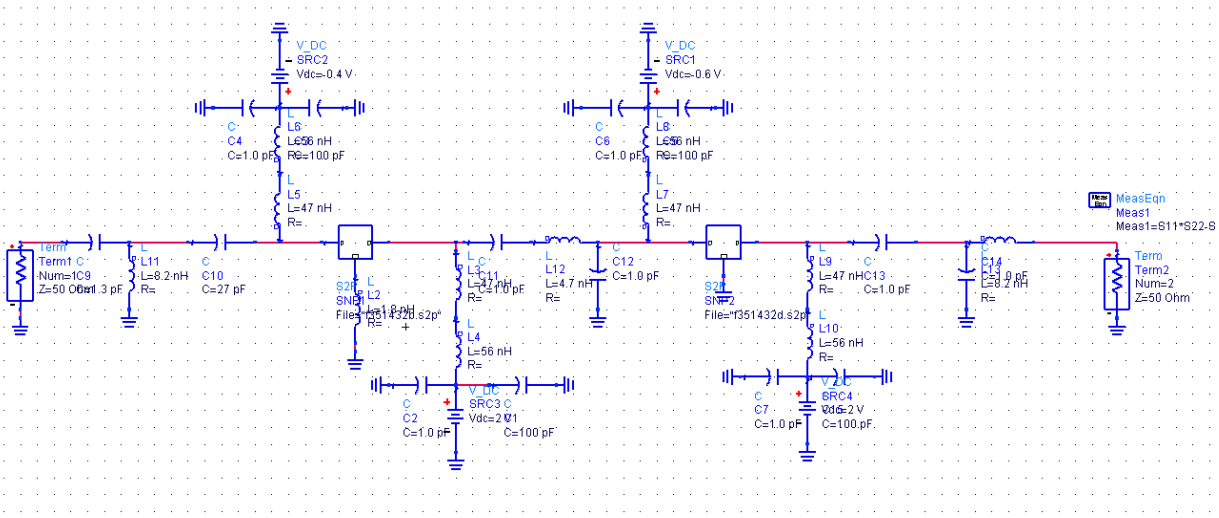

Figure 32 Final Schematic of LNA with Real Components

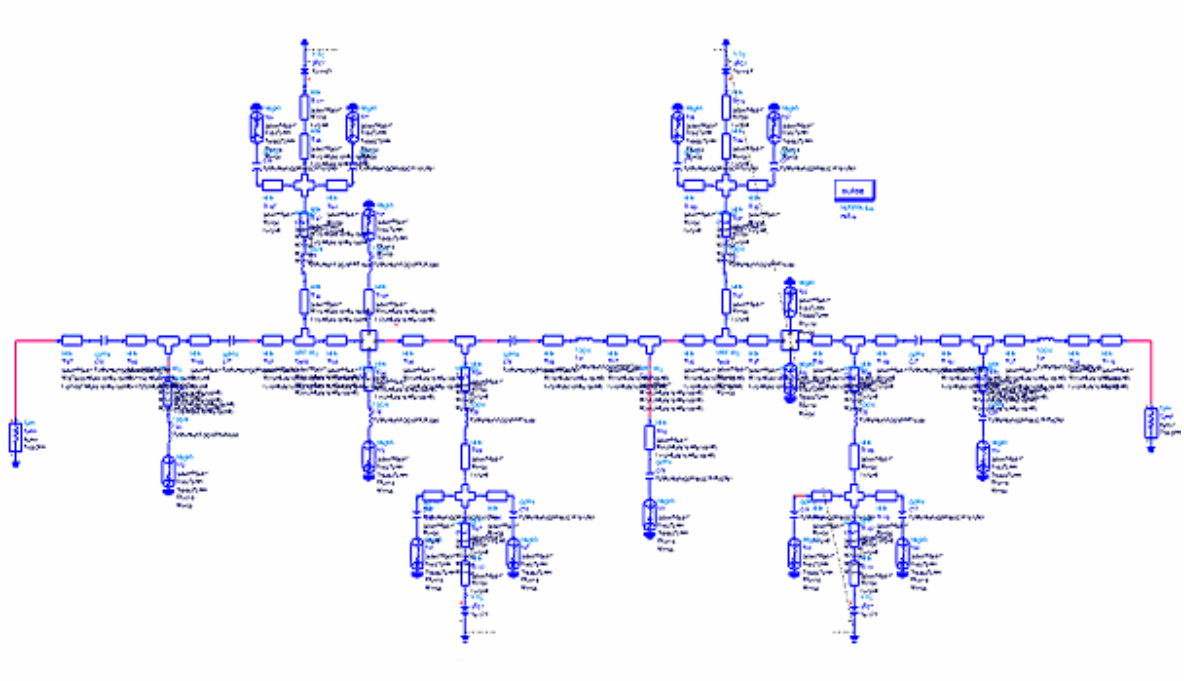

Figure 33 LNA Final Layout Schematic for Two Stage LNA with Microstrip Line

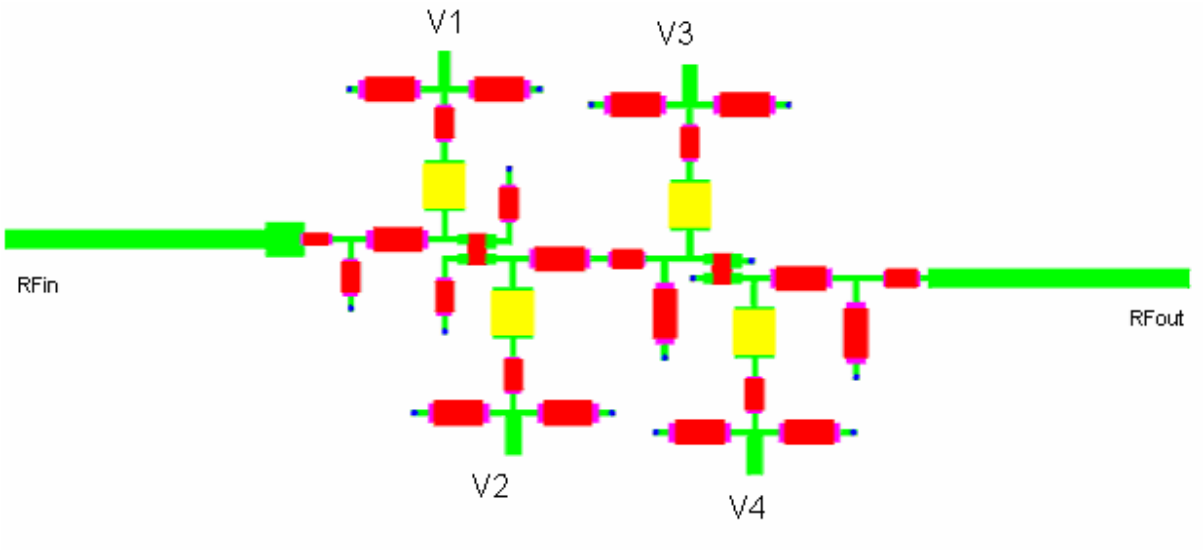

Figure 34 LNA Final Layout

Where
RFin = Input signal
RFout = Output signal
V_1 = Gate voltage (-0.64 V)
V_2 = Drain voltage (2 V)
V_3 = Gate voltage (-0.40 V)
V_4 = Drain voltage (2 V)

4.4.1 Simulation Results of Final Layout

The following Figure 35 to Figure 38 shows the simulated results of final layout of LNA with real components and all the graphs have taken from advanced design systems (ADS) software.

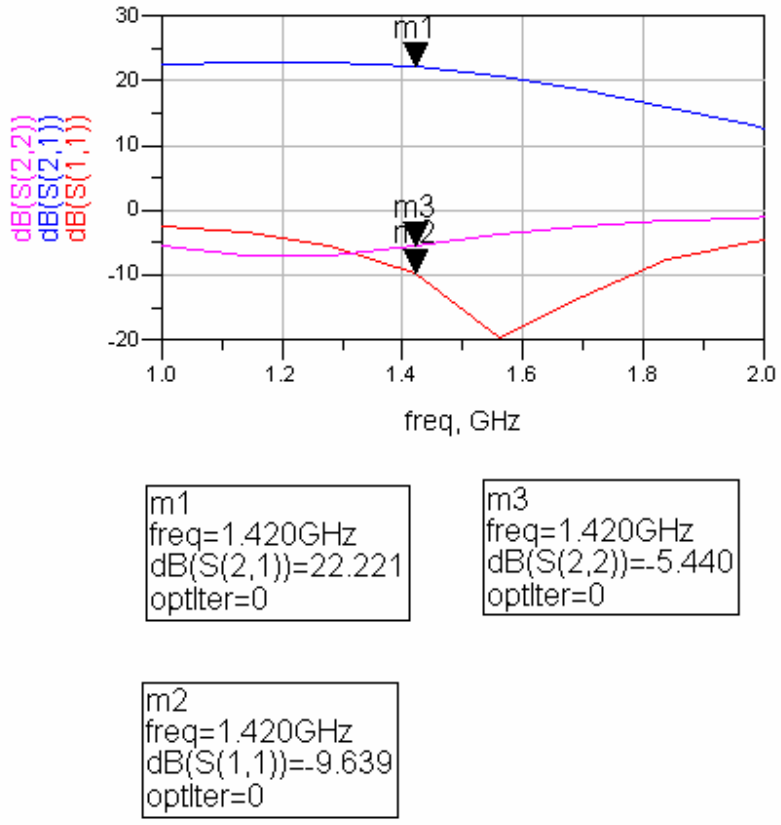

Figure 35 LNA Final Layout Schematic S-parameters

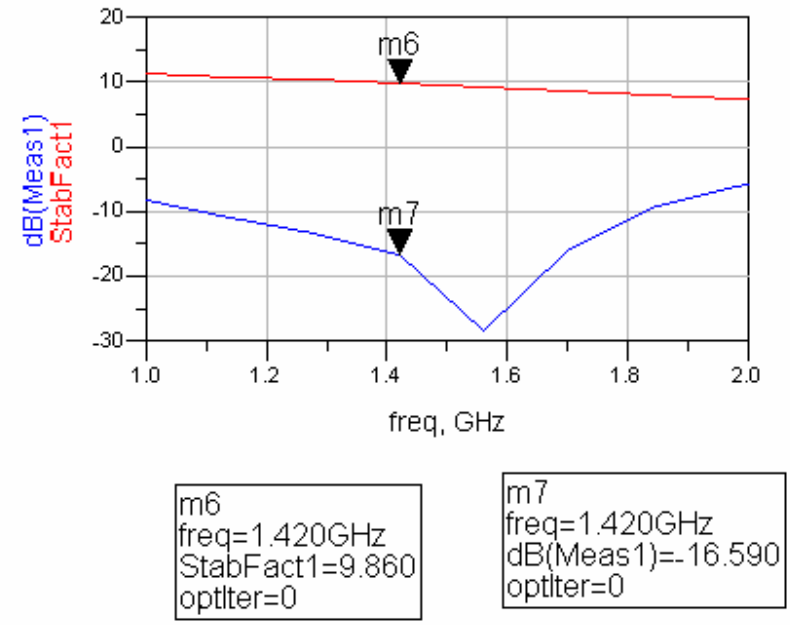

Figure 36 LNA Final Layout Schematic Stability Plot

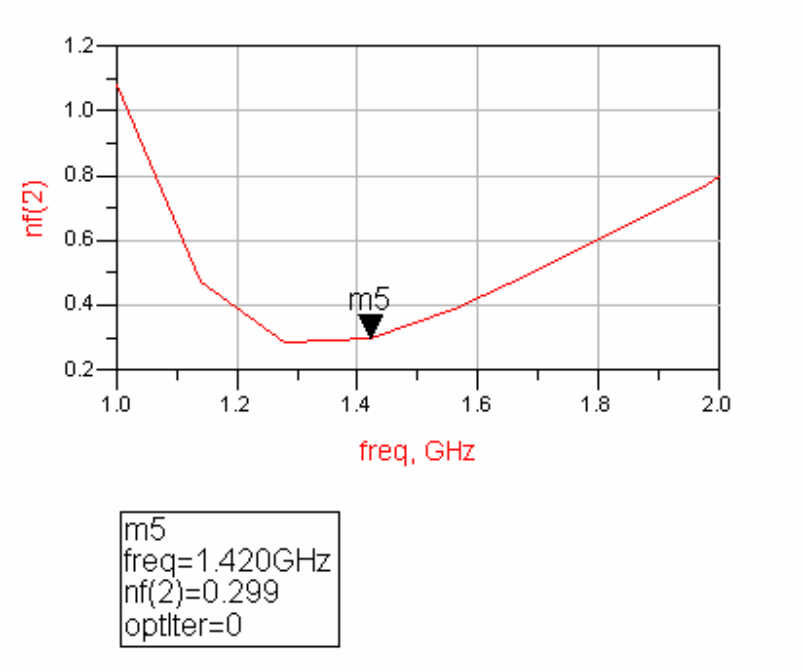

Figure 37 LNA Final Layout Schematic Noise Figure

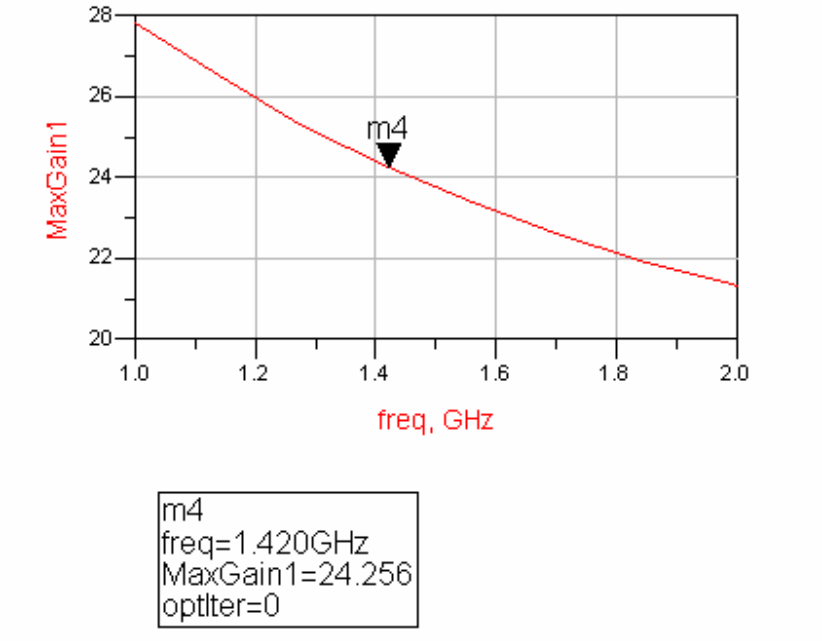

Figure 38 LNA Simplified Schematic Gain Plot

4.5 Comparing Results

In our designed L-band two stage LNA, we used GaAs technology for the Radio Astronomy application to provide low power, low cost, operational ability over a wide range of temperature, lower noise figure and higher gain. The sub circuits in this design are similarly related to traditional LNA but still there are few slight differences. We have selected Rogers R03003 material for fabrication because of its low dielectric loss at higher frequencies and in biasing we use bipolar power sources due to their low noise figure, high gain and high efficiency. From architecture point of view, inductive degeneration architecture is used in our LNA design and finally the most important difference from other researches on LNA is that, our two stage LNA at 1.42 GHz is designed to connect, match and test together with the patch antenna used in Radio telescope systems.

In all radio telescopes, the sensitivity is the main important parameter to consider because the sensitivity of the radio telescope is used to effectively detect the weak natural radio emissions coming from the galaxies. So a noise figure is the most important parameter in radio telescope as the sensitivity is depending on its value, the smaller it is, the higher is the sensitivity of the telescope. From our simulation of two stage LNA, we achieved noise figure 0.299 dB and gain 24.25 dB. By comparing our results with LNA's explained in references **[13]**, **[14]**, **[15]**, the difference is that RC elements have been used in the others biasing networks and matching networks, while LC elements have been used in our biasing and matching networks. Using RC networks they achieve more stability with a relatively higher noise figure but the use of LC networks gives us a lesser noise figure and less stability. Comparing our achieved results from the other previously research works on LNA (Ref **[13]**, **[14]**, **[15])** shows that our project is much more efficient to the radio astronomy applications due to super low noise figure and high gain.

5

Fabrication and Test plan

5.1 Fabrication of LNA

To fabricate whole two stage low noise amplifier R03003 material was used because R03003 has low dielectric loss at high frequencies. For this particular fabrication of total design R03003 material with dielectric constant ε_r = 3, standard thickness (T) = 0.50 mm and standard copper cladding (U) = 17 µm was used. The data sheet of R03003 material is shown in appendix section.

In order to connect the RF input signal port and output port of Fabricated LNA board to the Network Analyzer, two SMA connectors at both input and output ports were used.

Initially the fabrication work was started by selecting a material R03003 with the components case size 0603 (1.52 X 0.76) mm**.** But after making a layout file which is used to fabricate all the components on the material, it was realized that it is very difficult to solder such small component case sizes. Therefore the component case sizes were changed to 1206 (3.2 X 1.6) mm in order to solder easily on the fabrication material. Now fabricated circuit is showing in Figure 39

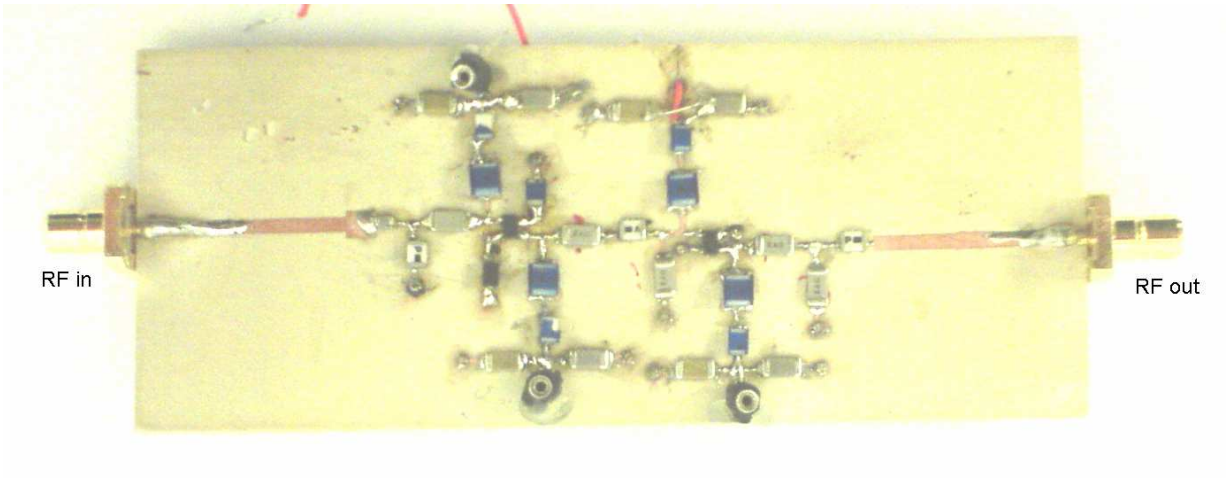

Figure 39 Fabricated Circuit

5.2 Test Plan

The final step of this project is to test the result of the circuit board of LNA. In the process of etching board bigger die size of all the components was used for soldering purpose and for measurement. For both RF input and RF output 50 ohms transmission line was used.

Before starting the measurement of LNA, first consideration was a dc level measurement. If there is any problem in dc levels it will affect the performance of the circuit board of LNA design.

In order to Test and Measure this fabricated two stage Low Noise Amplifier board, the following equipments are required.

- Power supply unit +7 V (dual power)
- Digital Multimeters
- Breadboard
- Connection wires
- Spectrum analyzer
- Network analyzer

Before going to Test the total two stages LNA, initially test was initiated by checking the bias point of an individual transistors separately on bread board.

Important precautions are to be considered before starting the measurement of LNA circuit board

- Before applying supply voltages to the transistor check all the connections carefully.
- Turn on the power supply unit
- Always start to apply the supply voltages from the gate side of the transistor slowly in steps of 0.1 V to required gate voltage.
- Slowly apply supply voltage to drain side of the transistor.

According to the DC simulations the Required Gate voltage is -0.64 V for (2 V, 10 mA) bias point in first stage and -0.39 V for (2 V, 30 mA) bias point in second stage respectively. To apply such bias voltages to the transistors precautions were to be made by providing a drain and gate resistors to the transistors. For this reason calculation of the resistor values according to two bias points of the two transistors were made, for first stage transistor the drain resistor is 200 Ω and gate resistor is 1.5 kΩ and for second stage the drain resistor is 66 Ω

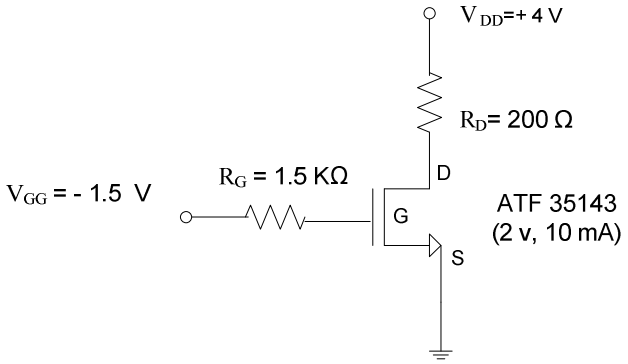

Figure 40 Bias Setup for a Single Transistor in First Stage

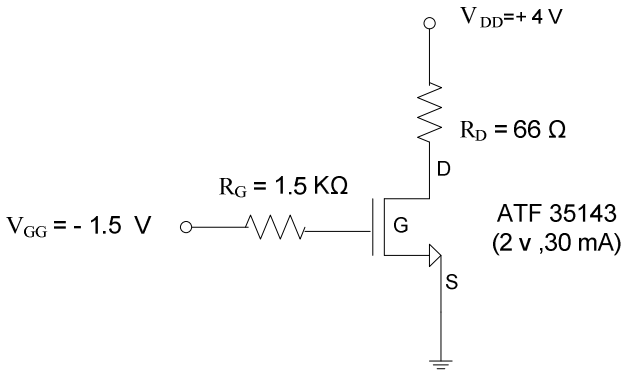

Figure 41 Bias Setup for a Single Transistor in Second Stage

Then initially the bias point test was started by applying gate voltage to the Gate side of transistor and then applied the required drain voltage to the drain of the Transistor from the dual power supply unit. But whenever two supply voltages to the transistor with above arrangement were applied, no stable bias point was achieved meaning that the required bias point voltages are fluctuating. It was further tested by a spectrum analyzer, which showed that the test circuit is oscillating.

Then it was decided to change the bias set up to get a stable bias point. For this an extra feedback resistor was used (from drain to gate side of transistor) in addition to the drain resistor and gate resistor. This arrangement is show in following figures

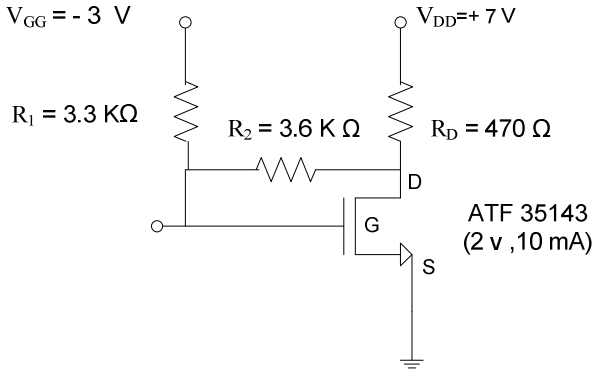

Figure 42 Bias Setup for First stage with Extra Feedback Resistor

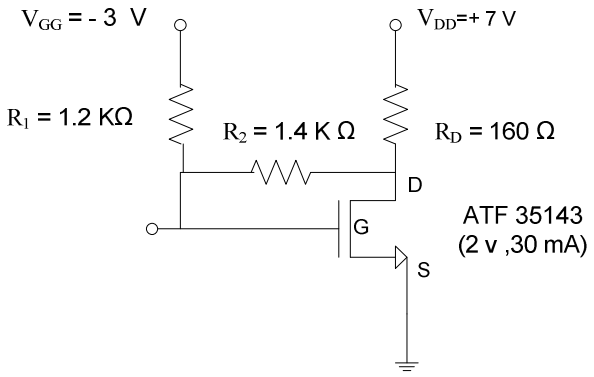

Figure 43 Bias Setup for Second stage with Extra Feedback Resistor

Once again the test was conducted but the outcome was the same. Again test was made with spectrum analyzer to check whether the circuit is oscillating or not and it showed that the circuit is still oscillating at lower frequencies like 149 MHz and 355 MHz for two stages respectively. There are some general reasons for unstable bias point they are listed below

- Due to long connecting wires in bread board arrangement for bias point selection which will acts as like oscillator at lower frequencies.
- Any improper soldering in test board.
- Inherent design problem

Then the circuit was trouble-shoot according to above mentioned points and was tested by spectrum analyzer, which showed that again it is oscillating the required bias point. Finally it was decided to check the other reason for oscillating, which included improper soldering. After re-soldering some components, the circuit was tested again by spectrum analyzer and it shows that the circuit was still oscillating. It was decided that this problem is due to the inherent design problem and the only solution is that redesign the circuit will rectify the problem. This task was not achieved because of time restraints.

6

Conclusions and Future Work

The main goal of this thesis was to design a two stage low noise amplifier for radio telescope system working at 1.42 GHz frequency to extract and amplify the received signals coming from galaxies. The thesis can be used for educational purpose in Halmstad University. Finally the designed LNA is to connect, match and test together with patch antenna to reduce the system components and signal loss.

The simulation results of the two stage low noise amplifier design and layout were successful and reached all the target specifications. In the proposal, the first stage was designed for low noise figure and second stage for high gain. From the simulation we got the noise figure 0.299 dB and gain 24.25 dB. While measuring the values from the fabricated circuit board, we found that bias point is not stable due to self oscillations in amplifier at lower frequencies like 149 MHz for first stage and 355 MHz for second stage. This problem was tackled in several ways but it did not work because of its inherent design problem.

For future work it is strongly recommended that special care is to be taken while connecting wires between components on the board and the voltage supply. Also effort to reduce the complexity of the circuit with fewer components would help. Another important point is tried to redesign the stability circuits at lower frequencies to make the circuits stable at lower frequencies. After that the designed two stage LNA can connect, match and test together with patch antenna.

During this time, we feel that we have gathered and studied enormous information on how radio telescopes and low noise amplifiers (LNA) works. For simulation, advanced design systems software was used but it was new for us. We learnt a lot of new tools from this software and used them in our design process. The best thing about this work has been our experience in doing a lot of practical work

Appendix

In this section, showing the datasheet of ATF 35143 transistor and the datasheet of material (Rogers RO3003) which is used for our fabrication process

Datasheets of ATF 35143

Freq. GHz	S_{11} Mag.	S_{11} Ang.	S_{21} dB	S_{21} Mag.	S_{21} Ang.	S_{12} dB	S_{12} Mag.	S_{12} Ang.	S_{22} Mag.	S_{22} Ang.	MSG/MAG dB
0.50	0.99	-18.75	15.89	6.23	164.76	-32.40	0.024	77.63	0.63	-14.09	24.14
0.75	0.97	-29.11	15.79	6.16	155.98	-28.87	0.036	70.58	0.61	-19.69	22.30
1.00	0.95	-38.28	15.61	6.03	148.42	-26.56	0.047	64.88	0.60	-26.10	21.08
1.50	0.91	-55.52	15.17	5.73	133.92	-23.61	0.066	54.16	0.57	-38.73	19.39
1.75	0.89	-63.78	14.92	5.57	127.01	-22.62	0.074	49.11	0.56	-44.79	18.75
2.00	0.86	-71.82	14.65	5.40	120.27	-21.72	0.082	44.08	0.54	-50.70	18.19
2.50	0.81	-87.59	14.11	5.08	107.36	-20.35	0.096	34.60	0.51	-61.95	17.23
3.00	0.76	-103.22	13.54	4.76	95.04	-19.41	0.107	25.71	0.47	-72.47	16.48
4.00	0.66	-134.81	12.40	4.17	71.95	-18.27	0.122	9.04	0.41	-91.47	15.34
5.00	0.61	-165.34	11.29	3.67	50.43	-17.65	0.131	-5.97	0.34	-110.05	14.47
6.00	0.58	165.88	10.27	3.26	30.28	-17.33	0.136	-20.15	0.27	-129.24	13.80
7.00	0.57	137.00	9.27	2.91	10.68	-17.14	0.139	-33.84	0.21	-150.49	13.21
8.00	0.58	110.78	8.33	2.61	-8.09	-17.14	0.139	-45.60	0.17	-174.77	12.73
9.00	0.61	86.75	7.32	2.32	-26.38	-17.20	0.138	-57.65	0.13	154.01	10.69
10.00	0.65	66.25	6.44	2.10	-43.90	-17.20	0.138	-68.22	0.11	118.18	9.85
11.00	0.69	46.88	5.54	1.89	-61.97	-17.27	0.137	-79.30	0.14	78.36	9.16
12.00	0.72	27.76	4.56	1.69	-79.90	-17.39	0.135	-90.87	0.19	49.57	8.34
13.00	0.74	8.62	3.45	1.49	-97.18	-17.79	0.129	-102.19	0.26	29.95	7.35
14.00	0.77	-5.28	2.33	1.31	-112.92	-18.20	0.123	-110.80	0.33	9.45	6.51
15.00	0.82	-16.03	1.29	1.16	-128.66	-18.56	0.118	-120.09	0.39	-7.98	6.51
16.00	0.82	-28.32	0.19	1.02	-144.87	-18.79	0.115	-129.92	0.45	-22.30	5.48
17.00	0.84	-40.43	-0.87	0.91	-159.49	-18.79	0.115	-139.60	0.51	-32.23	5.24
18.00	0.86	-56.14	-1.99	0.80	-175.19	-19.33	0.108	-149.17	0.57	-44.43	4.72

Table 5 Scattering Parameters of ATF 35143 Transistors (V_{DS} = 2 V, I_{DS} = 10 mA) **[24]**

Freq. GHz	F_{min} dB	Γ_{opt} Mag.	Ang.	$R_{n/50}$ -	G_a dB
0.5	0.10	0.88	5.0	0.15	20.5
0.9	0.11	0.84	14.0	0.15	19.0
1.0	0.12	0.83	16.0	0.15	18.6
1.5	0.17	0.77	26.0	0.15	17.5
1.8	0.20	0.74	31.9	0.15	16.9
2.0	0.23	0.71	37.3	0.14	16.4
2.5	0.29	0.66	48.6	0.14	15.7
3.0	0.34	0.60	60.6	0.12	15.0
4.0	0.46	0.52	86.8	0.12	13.6
5.0	0.58	0.45	115.3	0.08	12.4
6.0	0.69	0.40	145.8	0.05	11.3
7.0	0.81	0.37	177.7	0.05	10.3
8.0	0.92	0.35	-149.3	0.07	9.5
9.0	1.04	0.35	-115.6	0.12	8.8
10.0	1.16	0.37	-81.8	0.22	8.3

Table 6 Typical Noise Parameters of ATF 35143 **[24]**

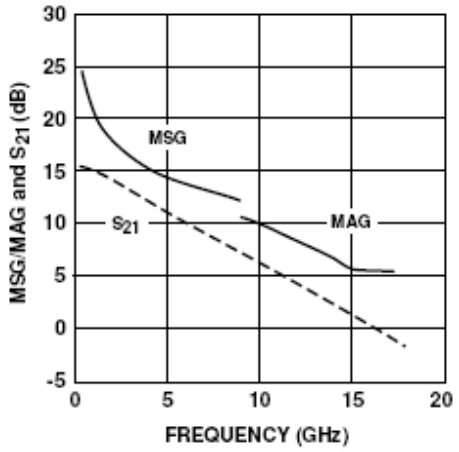

Figure 44 MSG/MAG and $|S_{21}|^2$ vs Frequency
at 2 V, 10 mA **[24]**

Freq. GHz	S_{11} Mag.	S_{11} Ang.	S_{21} dB	S_{21} Mag.	S_{21} Ang.	S_{12} dB	S_{12} Mag.	S_{12} Ang.	S_{22} Mag.	S_{22} Ang.	MSG/MAG dB
0.50	0.99	-20.95	18.17	8.10	163.18	-33.56	0.021	77.39	0.49	-15.99	25.87
0.75	0.96	-32.34	18.02	7.96	153.79	-30.17	0.031	70.55	0.47	-22.00	24.10
1.00	0.94	-42.36	17.77	7.73	145.67	-27.96	0.040	65.08	0.46	-29.03	22.86
1.50	0.88	-61.09	17.18	7.22	130.36	-25.04	0.056	54.79	0.43	-42.64	21.11
1.75	0.85	-69.98	16.85	6.96	123.20	-24.01	0.063	50.12	0.41	-48.96	20.42
2.00	0.82	-78.53	16.50	6.69	116.28	-23.22	0.069	45.58	0.39	-55.19	19.86
2.50	0.76	-95.14	15.81	6.17	103.17	-21.94	0.080	37.15	0.36	-66.91	18.87
3.00	0.70	-111.48	15.11	5.69	90.88	-21.01	0.089	29.29	0.34	-77.74	18.06
4.00	0.61	-143.89	13.73	4.86	68.24	-19.83	0.102	14.76	0.28	-97.29	16.78
5.00	0.56	-174.55	12.46	4.20	47.48	-19.02	0.112	1.63	0.23	-117.24	15.74
6.00	0.55	157.19	11.31	3.68	28.10	-18.49	0.119	-10.98	0.17	-139.78	14.90
7.00	0.55	129.18	10.22	3.24	9.28	-18.13	0.124	-23.67	0.13	-169.09	14.17
8.00	0.56	104.19	9.20	2.88	-8.75	-17.79	0.129	-34.72	0.11	155.22	11.98
9.00	0.60	81.48	8.15	2.56	-26.37	-17.59	0.132	-46.33	0.11	112.23	10.82
10.00	0.64	62.07	7.24	2.30	-43.37	-17.33	0.136	-57.43	0.13	77.30	10.15
11.00	0.68	43.83	6.29	2.06	-60.90	-17.20	0.138	-68.78	0.18	51.74	9.51
12.00	0.72	25.46	5.27	1.84	-78.22	-17.14	0.139	-81.32	0.24	32.67	8.77
13.00	0.74	6.81	4.14	1.61	-94.88	-17.33	0.136	-93.11	0.31	17.81	7.87
14.00	0.77	-6.74	3.01	1.41	-110.07	-17.65	0.131	-103.06	0.38	0.45	7.08
15.00	0.82	-17.21	1.94	1.25	-125.15	-17.86	0.128	-112.88	0.43	-15.44	7.06
16.00	0.83	-29.31	0.87	1.11	-140.80	-18.06	0.125	-123.55	0.49	-29.37	6.13
17.00	0.85	-41.30	-0.15	0.98	-154.83	-18.13	0.124	-134.43	0.54	-38.55	5.89
18.00	0.87	-56.87	-1.24	0.87	-170.03	-18.56	0.118	-144.88	0.60	-49.70	5.39

Table 7 Scattering Parameters of ATF 35143 Transistors (V_{DS} = 2 V, I_{DS} = 30 mA) **[24]**

Freq. GHz	F_{min} dB	Γ_{opt} Mag.	Γ_{opt} Ang.	$R_{n/50}$ -	G_a dB
0.5	0.11	0.87	2.7	0.18	21.6
0.9	0.15	0.81	12.1	0.17	20.2
1.0	0.16	0.80	14.5	0.16	19.9
1.5	0.22	0.73	26.3	0.15	18.7
1.8	0.25	0.69	33.4	0.15	18.0
2.0	0.27	0.66	38.1	0.14	17.7
2.5	0.33	0.60	50.6	0.13	17.0
3.0	0.39	0.54	64.2	0.12	16.2
4.0	0.52	0.45	94.0	0.10	14.8
5.0	0.64	0.39	126.5	0.07	13.5
6.0	0.77	0.34	160.6	0.05	12.4
7.0	0.90	0.33	-164.7	0.06	11.4
8.0	1.02	0.33	-130.3	0.10	10.5
9.0	1.15	0.36	-97.5	0.18	9.7
10.0	1.28	0.40	-67.0	0.30	9.1

Table 8 Typical Noise Parameters of ATF 35143 Transistors **[24]**

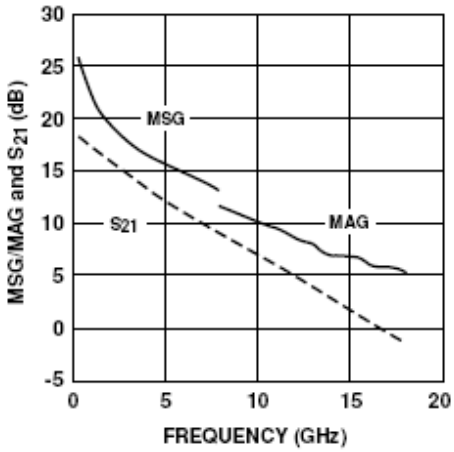

Figure 45 MSG/MAG and $|S_{21}|^2$ vs. Frequency at 2 V, 30 mA **[24]**

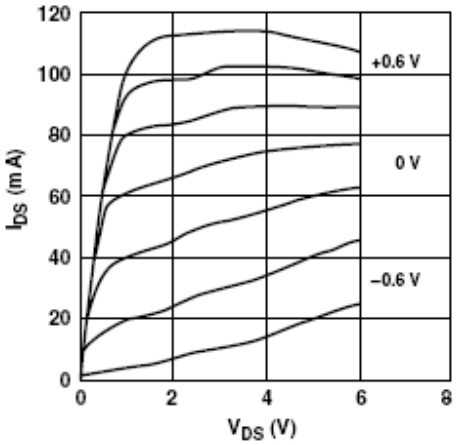

Figure 46 V_{DS} vs I_{DS} Curve **[24]**

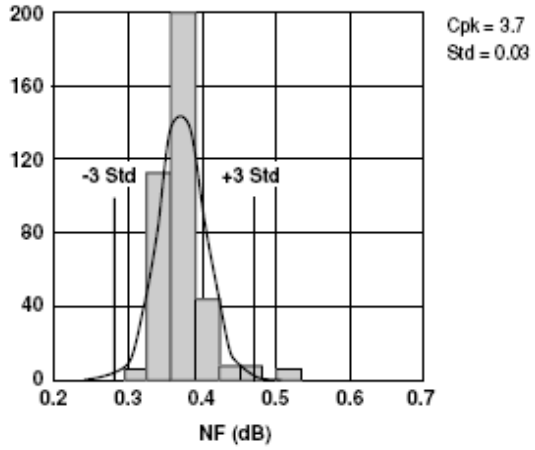

Figure 47 Noise Figure Charts **[24]**

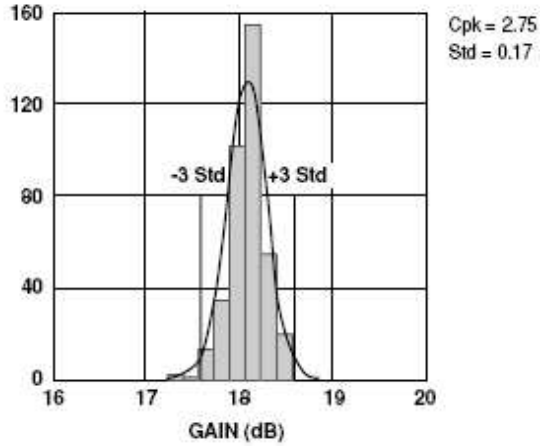

Figure 48 Gain Charts **[24]**

Datasheet of Rogers's (RO3003) Material

Typical Values — RO3000® Series High Frequency Laminates

PROPERTY	TYPICAL VALUE (1)			DIRECTION	UNIT	CONDITION	TEST METHOD
	RO3003	RO3006	RO3010				
Dielectric Constant ε_r	3.00±0.04(2)	6.15±0.15	10.2±0.30	Z	-	10GHz 23°C	IPC-TM-650 2.5.5.5
Dissipation Factor	0.0013	0.0020	0.0023	Z	-	10GHz 23°C	IPC-TM-650 2.5.5.5
Thermal Coefficient of ε_r	13	-160	-280	Z	ppm/°C	10GHz 0-100°C	IPC-TM-650 2.5.5.5
Dimensional Stability	0.5	0.5	0.5	X,Y	mm/m	COND A	ASTM D257
Volume Resistivity	10^7	10^3	10^3		MΩ•cm	COND A	IPC 2.5.17.1
Surface Resistivity	10^7	10^3	10^3		MΩ	COND A	IPC 2.5.17.1
Tensile Modulus	2068 (300)	2068 (300)	2068 (300)	X,Y	MPa (kpsi)	23°C	ASTM D638
Water Absorption	<0.1	<0.1	<0.1	-	%	D24/23	IPC-TM-650 2.6.2.1
Specific Heat	0.93 (0.22)	0.93 (0.22)	0.93 (0.22)		J/g/K (BTU/lb/°F)		Calculated
Thermal Conductivity	0.50	0.61	0.66	-	W/m/K	100°C	ASTM C518
Coefficient of Thermal Expansion	17 24	17 24	17 24	X,Y Z	ppm/°C	-55 to 288°C	ASTM D3386-94
Td	500	500	500		°C TGA		ASTM D 3850
Color	Tan	Tan	Off White				
Density	2.1	2.6	3.0		gm/cm³		
Copper Peel Strength	3.1 (17.6)	2.1 (12.2)	2.4 (13.4)		N/mm (lb/in)	After solder float	IPC-TM-2.4.8
Flammability	94V-0	94V-0	94V-0				UL
Lead-Free Process Compatible	Yes	Yes	Yes				

Table 9 Typical Value of RO3003 Material **[25]**

Here final schematic of low noise figure are divided into several parts

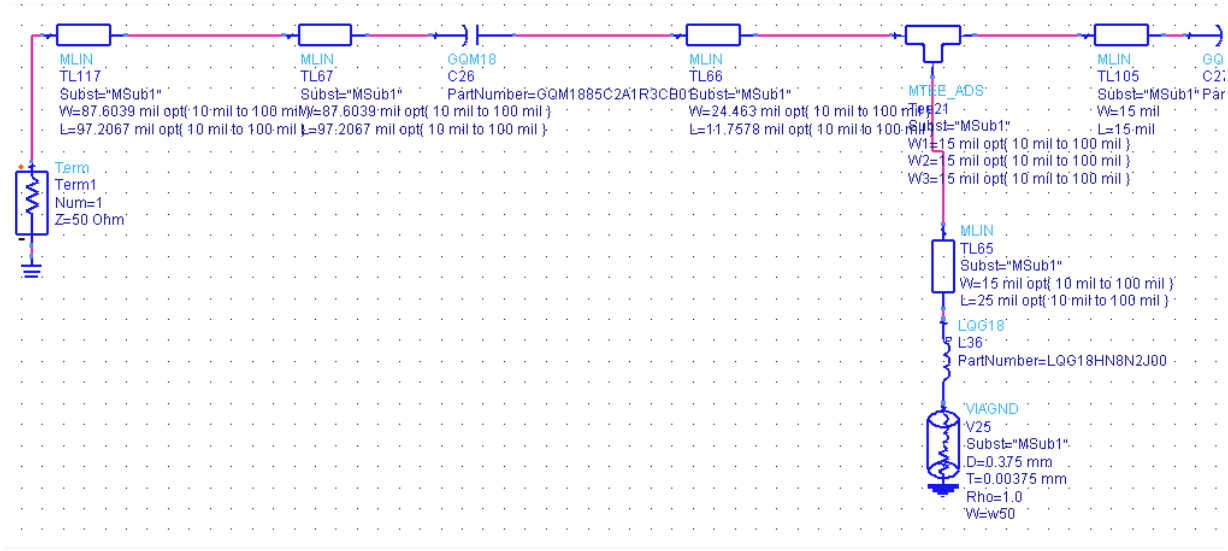

Figure 49 Parts 1 of Final Schematic

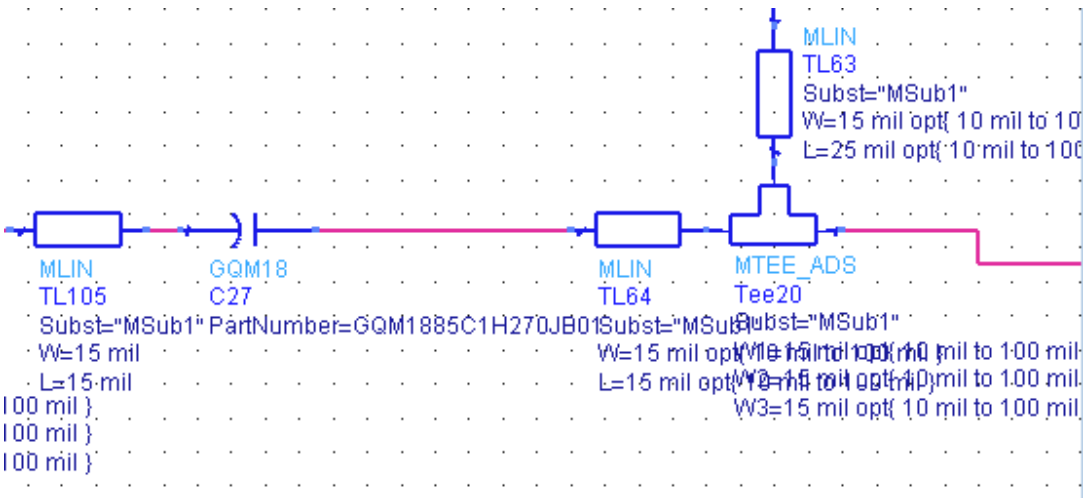

Figure 50 Part 2 of Final Schematic

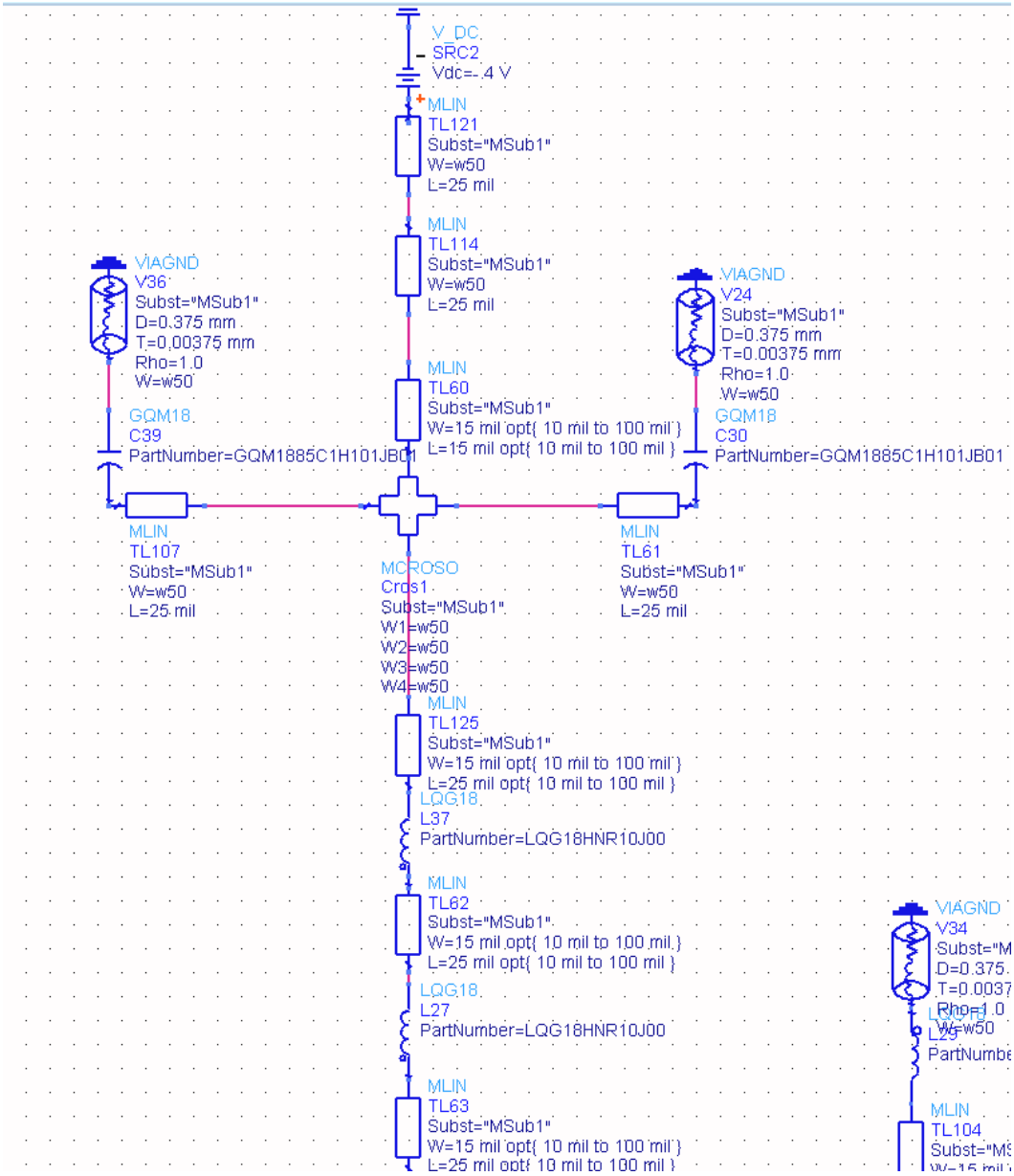

Figure 51 Part 3 of Final Schematic (Biasing Section)

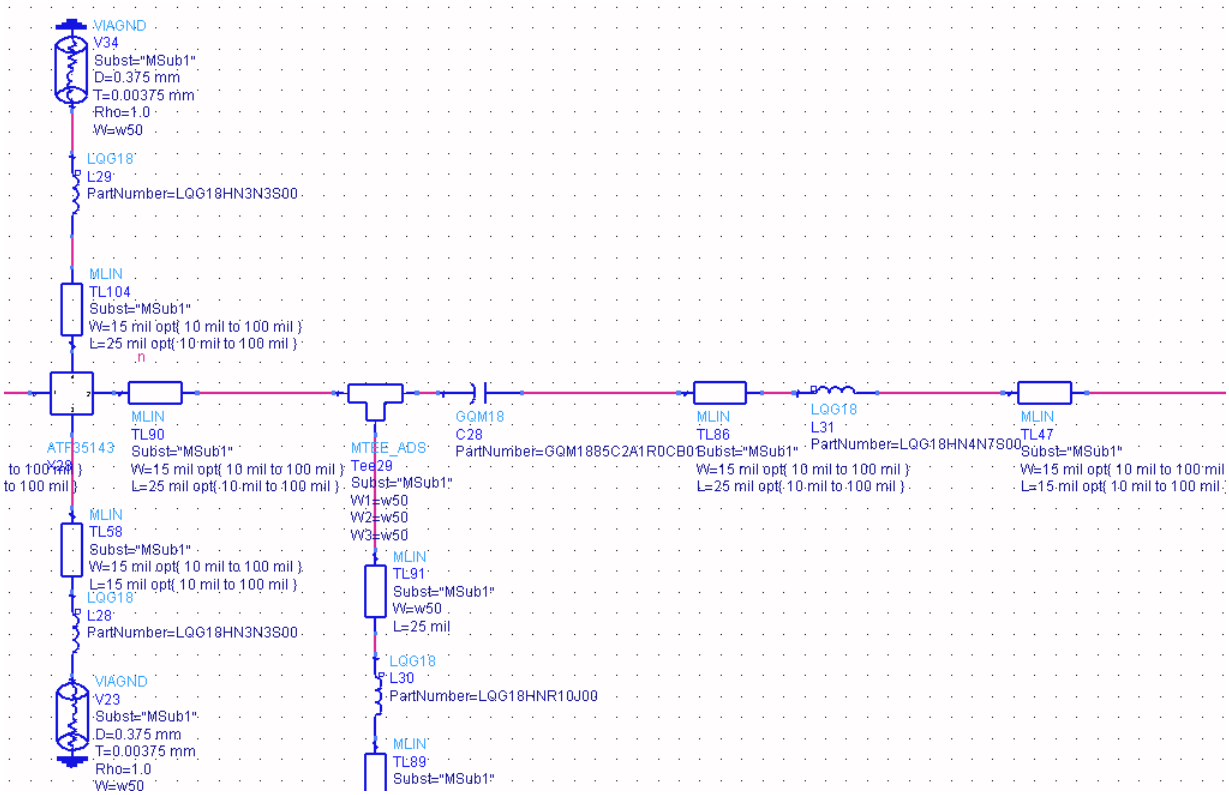

Figure 52 Parts 4 of Final Schematic

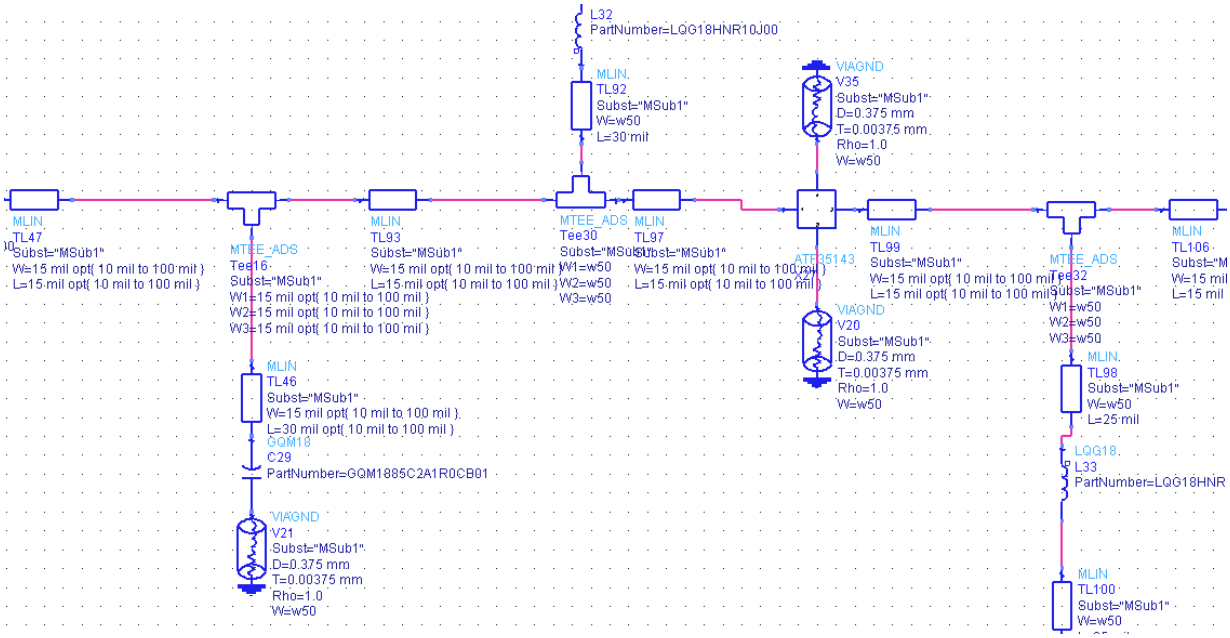

Figure 53 Parts 5 of Final Schematic

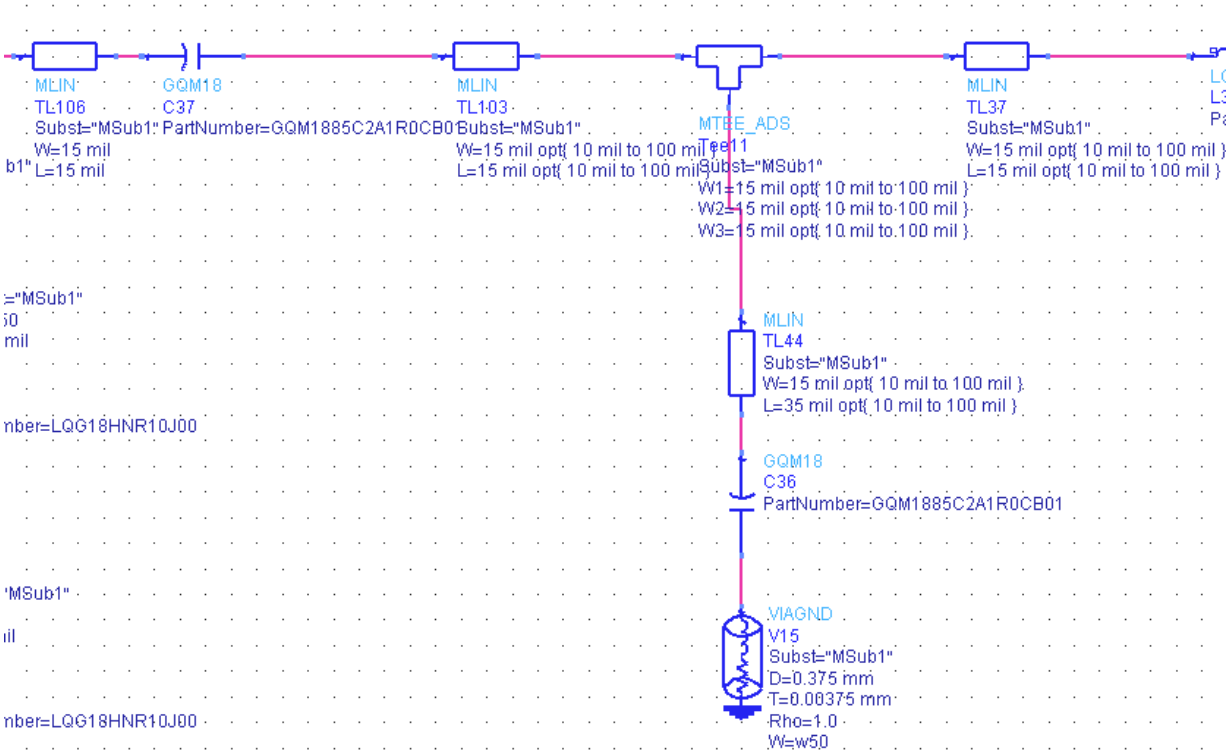

Figure 54 Part 6 of Final Schematic

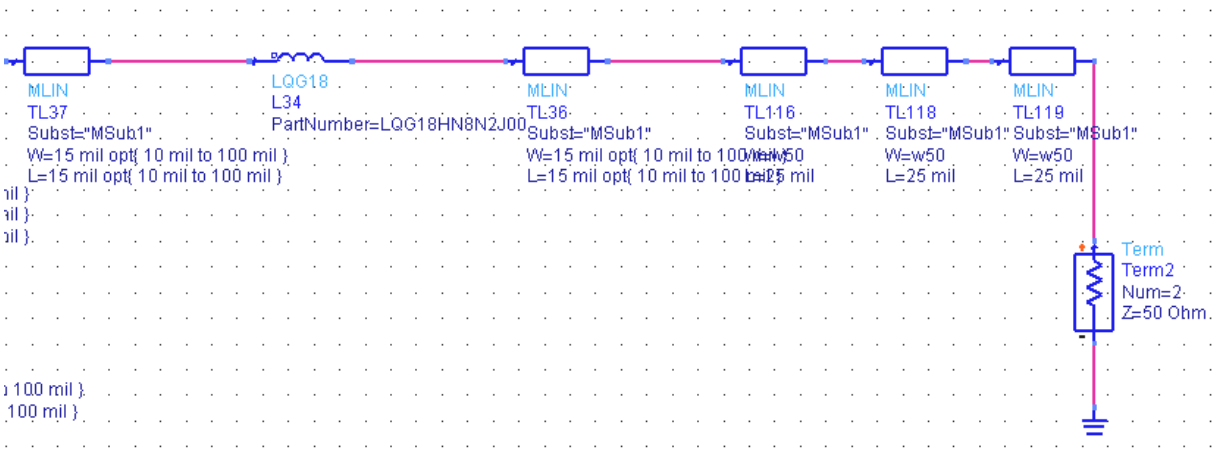

Figure 55 Part 7 of Final Schematic

Abbreviations

FET	Field effect transistor
PHEMT	Pseudomorphic high electron-mobility-transistor
HEMT	High Electron Mobility Transistor
LNA	Low Noise Amplifier
S_{11}	Input reflection coefficient
S_{12}	Reverse transmission gain
S_{22}	Output reflection coefficient
$S_{21 =}$	Forward gain
GaAs	Gallium arsenide
MESFET	Metal-Semiconductor Field Effect Transistor
MMIC	Monolithic Microwave Integrated Circuit
PC	Personal computer
PDA	Personal digital assistant
ADS	Advanced design systems

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